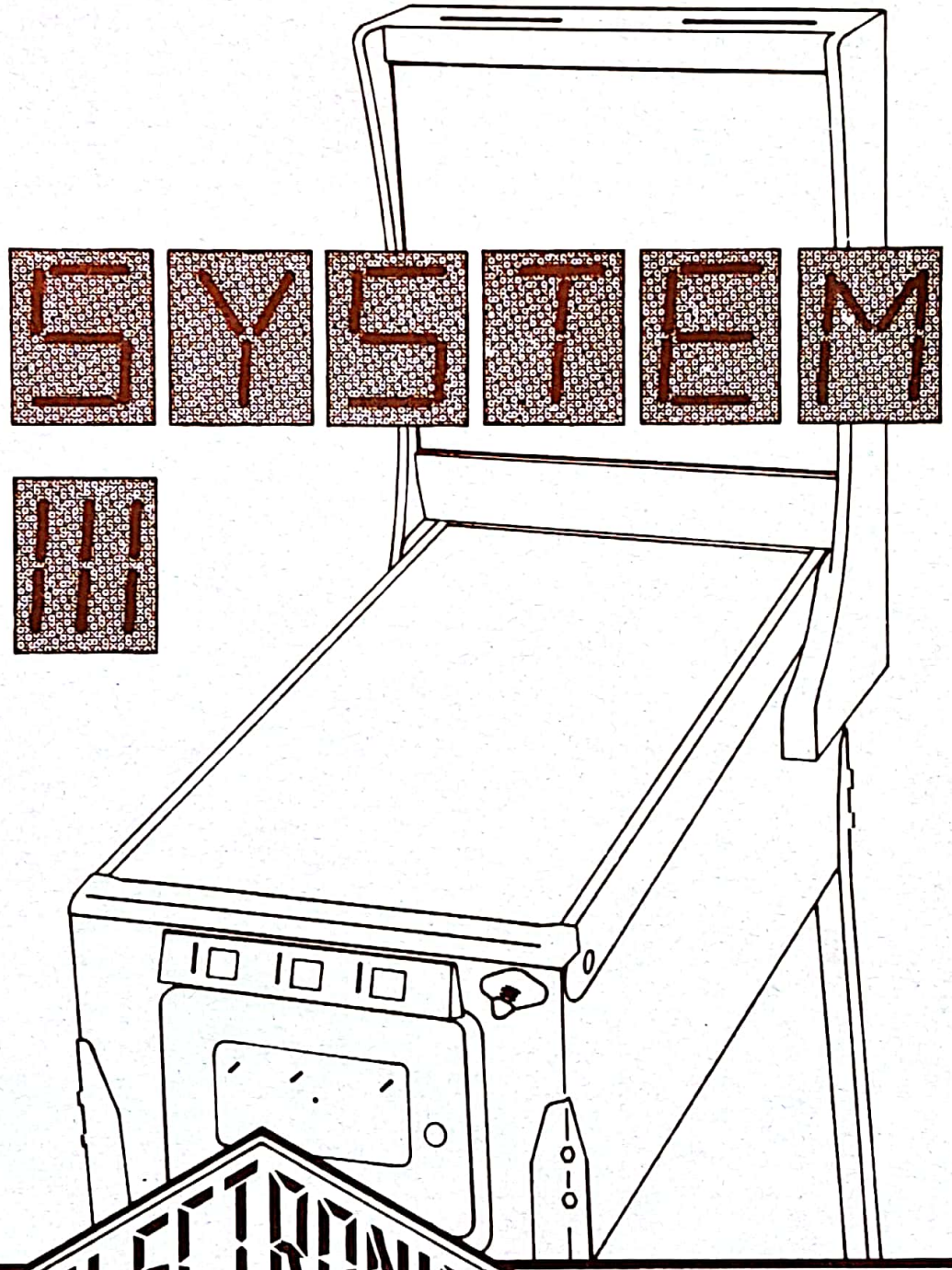
EURO

RECEL SPAIN S.A.
Manufactured in Madrid

FLIP

SYSTEM 80



ELECTRONIC SYSTEM

GENERAL INFORMATION

ELECTRONICS DIVISION

DOCUMENT NR Ø35-621

REV Ø2

MARCH-1.978

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MR. OPERATOR

We would advise you of the importance of reading this Manual, which will help you to obtain the very best efficiency in our electronic Pin–Ball.

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SECTION 1

GENERAL INFORMATION

1.1 FOREWORD

"SYSTEM III" represents the most advanced application of electronics technology in the pin-ball industry. Its performance betters all previous system possibilities with surprising simplicity, offering in addition such a quantity of information that opens up a new era in the coin operated games, thus allowing a strict and programmed control over the performance of every machine in all aspects (coin collection, faults, game behaviour, timing, etc).

All the information supplied by the machine (which is printed out) can be fed into a main computer, which will file and process all data, giving out percentages, averages, statistics, and which will activate an alarm when some parameter suffers a deviation greater than the set values.

With "SYSTEM III" we have obtained a pin-ball in which all units are interchangeable from one model to another, irrespective of whether it is a single, two or four player version. The only differences you will find between one model and another are the following: (1) the playfield; (2) the actual decoration; and (3) the game memory (which is mounted in the Master Unit, with socket).

1.2 PURPOSE OF THIS MANUAL

In this Manual we have described the characteristics, handling and maintenance of our "SYSTEM III". It has been written with existing pin-ball technical staff in mind, who might not yet be familiar with micro-processor technology.

This manual is intended to give a very simple understanding of our "SYSTEM III" and its general application to pin-ball machines, and here we are not going to deal with the particular characteristics of any given model, as these will be given in the respective service manual.

1.3 LAYOUT OF THE MANUAL

The contents of sections 2, 3, 4, 5, 6 and 7 are as follows :

Section 2 : Basic Concepts, is the heading for an elementary and brief introduction to the microprocessor technology. Its only purpose is to provide some general guide-lines to those technicians who have not yet come into contact with data processing electronic systems.

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Section 3 : Describes the main characteristics of the System: Self-Check, Representation areas, Handicaps, Adjustment, Logic Detector, Mini-printer and Simulation System.

Section 4 : This section is dedicated to an analysis of the essentially electrical parts: coils, lamps and contacts. It also includes a general schematic of the System.

Section 5 : This comprises a full description of all the units within the System, an explanation of the functioning of each of these units and theoretical, practical and connection diagrams for such units.

Section 6 : This presents a basic time diagram for the LSI MOS and RAM C-MOS chips, as well as the PIN-OUT for all the chips and components used.

Section 7 : This is firstly a map summarising the organization of the RAM memory, and a representation in full detail of all the display indications in the various representation areas.

1.4 GENERAL CHARACTERISTICS

* Processor in use: ROCKWELL PPS-4
* Intelligent system assembled on just 1 (one) module.
* General wiring system: flat tape
* Data memory maintained when the machine is switched off
* 4 counters of $6\frac{1}{2}$ digits
* Different handicap (highest score) for each player
* 3 and 5 balls
* 3 adjustable coin rejectors
* Electronic digital sound
* 2 types of game with extra play
* 3 types of game with extra ball
* Limit on extra play = 9 (separate from credit display)
* Limit on extra ball = 9 (with display for this use)
* Credit limit adjustable from 9 through 99
* Electronic match number
* Adjustments and rules contained in memory (without switches)
* Model and serial number register

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* Register code of the last printer used for coin collection
* Date or number register of last coin collection
* "Game Over" time register
* "Machine in Play" time register
* Coin meter for 1st coin rejector
* Coin meter for 2nd coin rejector
* Coin meter for 3rd coin rejector
* Extra Ball meter
* Extra Game meter
* Total Service meter
* Total Play meter
* 4 extra meters for use in the game or for any other use
* Display representation of all the above mentioned data
* Print-out of all data on portable mini-printer
* Charge and/or zeroing of registers and meters with mini-printer
* Data collected with mini-printer can be fed to central computer
* Cabinet with "fold-down" head (without disconnecting)
* All units interchangeable from one model to another
* Alteration and/or zeroing of registers and meters by printer
* Power supply (adjustable): 100-120-135-150-200-220-240-260 v. (50 - 60 Hz)
* Consumption: 110 watts (at rest)
  280 watts (maximum, in play)
* Playfield inclination: 5° - 10° (adjustable)
* Dimensions when mounted: 1190 mm deep
  650 mm wide
  1780 mm high
* Dimensions in transport: 1315 mm deep
  670 mm wide
  580 mm high
* Nett weight: 91 kgs.
* Gross weight: 105 kgs.

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1.5 EXPRESSIONS

In order to understand this Manual more easily, we define herebelow some of the principal terms and expressions.

Ø (Low)	Logic level of a power point or register $R \leq 0{,}6$ volts
1 (High) ...	Logic level of a power point or register $R \geq 3$ volts
OPEN	Logic level between High and Low
PULSE	Interval from which a level changes to another and returns to the original level
SET	Line, instruction or fact of setting "HIGH" in a point or register
RESET	Line, instruction or fact of setting "LOW" in a point or register
CLOCK	Line with repetitive pulses used as a time base, or pulse that defines the instant when an effect should take place
ENABLE	Form of allowing something to realize a certain function
DATA	Line or lines via which data are transmitted or received
BUS	Group of lines used by all the circuits connected to it
BUFFER	Chips used as protection and interface between the MOS circuits and the TTL and Drivers. $f = A$
INVERTER ...	Chip whose logic function is defined by $f = \overline{A}$
AND	Chip whose logic function is defined by $f = A.B.C.-.-.-$
NAND	Chip whose logic function is defined by $f = \overline{A.B.C.-.-.-}$
OR	Chip whose logic function is defined by $f = A + B + -$
NOR	Chip whose logic function is defined by $f = \overline{A + B + -}$
INTERFACE ..	Circuit which makes two different circuits compatible in level or form of working
RAM	Random Access Memory (variable data)
ROM	Read Only Memory (instructions and constants)
EPROM	Electric Programmable Read Only Memory
CPU	Central Processing Unit
DRIVER	Output interface (generally 1 transistor)
TTL	Transistor (IN) Transistor (OUT) Logic
PMOS	Positive Metal Oxide Semiconductor
NMOS	Negative Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input-Output
PIO	Programmable Input-Output
GPKD	General Processor Keyboard and Display
BIC	BUS interface circuit

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SECTION 2

BASIC CONCEPTS

2.1 SIMPLIFIED STRUCTURE

Basically the most simple lay-out involving a micro-processor system will be as depicted in the block diagram shown below :-

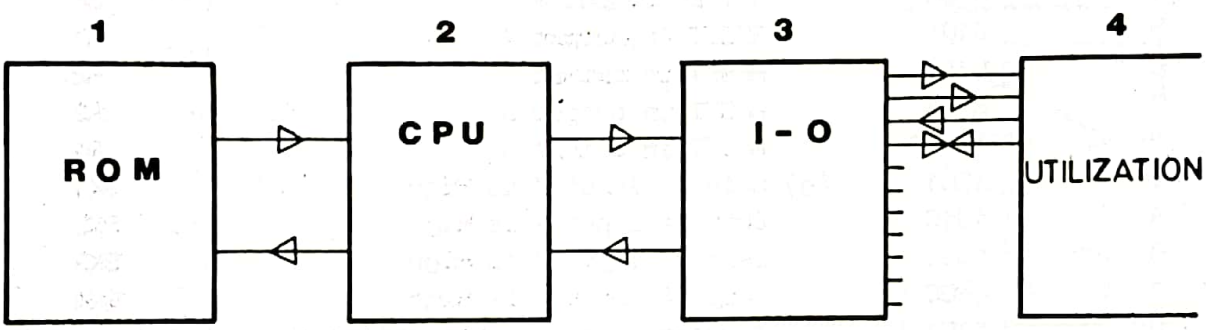

Fig. 2.1

The operation of such a system would be equivalent to a sequence circuit in which a control circuit 2 (CPU) alters the outputs from 3 (I/O) in accordance with a stored sequence in the program memory 1 (ROM).

The circuit 1 program memory contains the code for all those instructions received in circuit 2 (CPU), by which means it is able to process the data and transfer the results to circuit 3 (I/O) which in turn controls the coils, lamps and/or other parts of the system (4).

In order to see more clearly the basic operation, let us assume a very simple micro-processor system, as illustrated in Fig. 2.1 :

Chip Nº 1 (ROM) contains the combinations (or codes of 4 bits for example) that Chip Nº 2 (CPU) receives in sequence, bearing in mind that Chip Nº 1 is controlled by the same CPU (logic unit which interprets the instructions contained in ROM, and carries them out controlling the memories and peripherals). These codes are recorded, logically in binary, and each set of them (each word or 'byte') expresses a specific instruction.

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Chip Nº 2 (CPU) interprets each one of these combinations (instructions) and makes a SET, RESET or READING of any input from circuit 3 (I/O).

As each word (or byte) sent by the ROM to the CPU, contains 4 bits, there are 16 possible and different combinations (instructions) which are as follows :-

HEXAD.	INSTRUCTION	CPU FUNCTION	MNEMONIC
Ø	0000	SET in all outputs	S0
1	0001	SET in output 1	S1
2	0010	SET in output 2	S2
3	0011	SET in output 3	S3
4	0100	SET in output 4	S4
5	0101	RESET in output 1	R1
6	0110	RESET in output 2	R2
7	0111	RESET in output 3	R3
8	1000	RESET in output 4	R4
9	1001	(*) Skip if input 1 is High	SK1
A	1010	Skip if input 2 is High	SK2
B	1011	Skip if input 3 is High	SK3
C	1100	Skip if input 4 is High	SK4
D	1101	Advance as many instructions as indicated by the following word	
E	1110	Go back as many words as per the value of the following instruction	T+X T-X
F	1111	RESET all outputs	R0

(*) Ignore the following instruction if the given condition is complied with (Skip).

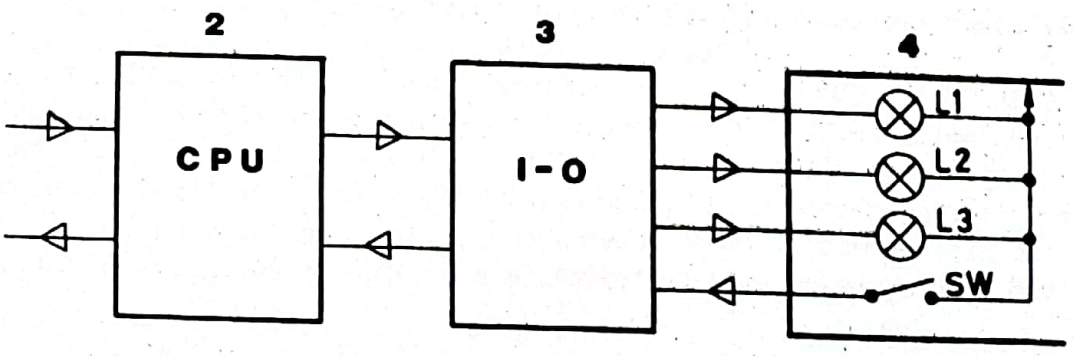

Fig. 2.2

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Assuming that we have this simplified system, we can now use it in the set-up shown under Fig. 2.2, and can make the following program.

The program will lite up the first lamp on pressing the switch (in 4) for the first time, the 2nd lamp will be lit up after pressing the switch for the second time, and with the 3rd press all three lamps will be flashing.

```
INIT   R0       Reset all outputs
       SK4      Has the switch been pressed?
       T-1
       SK4
       T+2  YES
       T-2
       S1       Lite up lamp 1
       SK4      Has the switch been pressed?
       T-1
       SK4
       T+2  YES
       T-2
       S2       Lite up lamp 2
       SK4      Has the switch been pressed?
       T-1
       SK4
       T+2  YES
       T-2
       S0       Set all outputs
       R0       Reset all outputs
       T-2
```

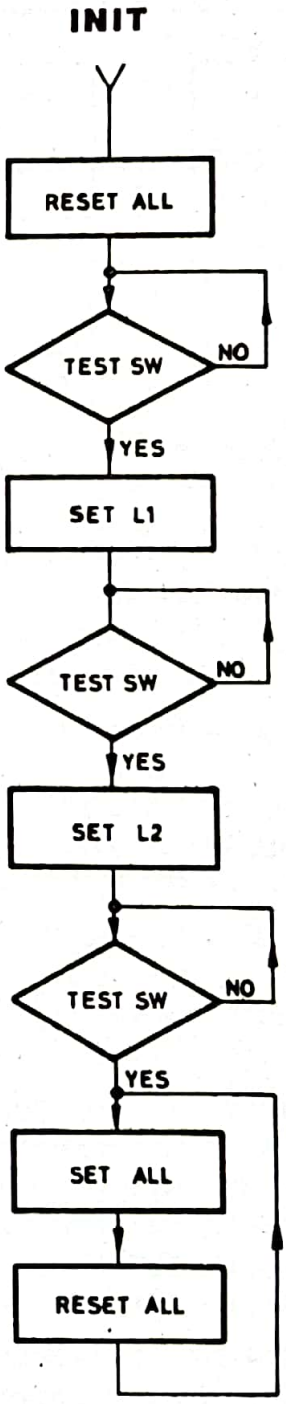

Fig. 2.3

With these instructions translated into binary code (according to the previous table) and recorded in the ROM memory, the program will carry out the prescribed steps, liteing up L1, then L2 and then flashing all 3 lamps.

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2.2 REAL BASIC STRUCTURE

We can now consider the real structure of a simple system using microprocessors (Fig. 2.4); here we have also added something new - the RAM memory.

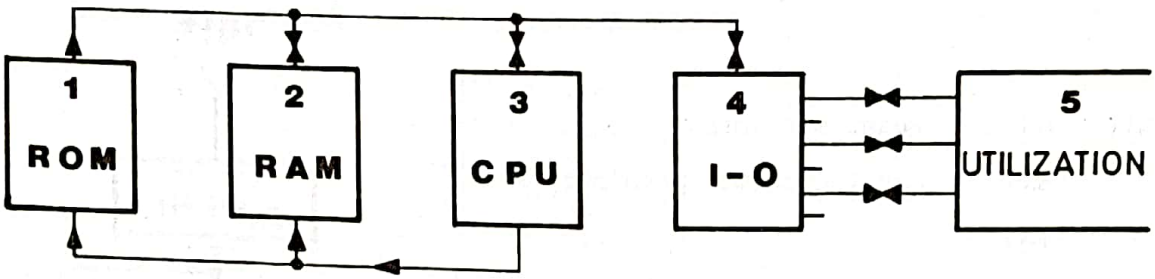

Fig. 2.4

Analysis of the system :

ROM (1) - Read Only Memory contains the program which is interpreted by the CPU which in turn will make or introduce data into the RAM memory or alter and read the inputs and outputs from the I/O (4), controlling by these latter, all the parts in UTILIZATION (5) (e.g. relays, motors, lamps, etc.). The ROM memory is recorded during manufacture and cannot be changed.

RAM (2) - Random Access Memory is the memory that the CPU uses to store all types of data (final or intermediate), subsequently making operations or alterations on the data and transferring these to the I/O outputs during the program run. This memory serves therefore as a variable data store for the CPU because this unit requires a large data stock capacity.

CPU (3) - Central Processing Unit interprets the program and carries out all the operations and movements indicated in the program. The CPU incorporates registers, accumulators, counters, decoders and multiplexers required to control and direct the memories and peripherals.

I/O (4) - Input/Output, a circuit which controls the external systems (indicators, motors, read-out and other peripherals) as directed by the CPU. Depending on the number of lines that the Utilization section (5) requires, there will be a need for the same number (1, 2 or "x") of I/O circuits (peripherals). These circuits can provide lines that would be outputs, inputs and both at the same time.

UTILIZATION (5) - This is an assembly of all those parts which the system needs in particular to operate. These parts could be other electronic circuits, read-outs or electrical or electromechanical receivers, loads of any type (with their drivers and respective interfaces) etc. etc.

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2.3 REAL STRUCTURE

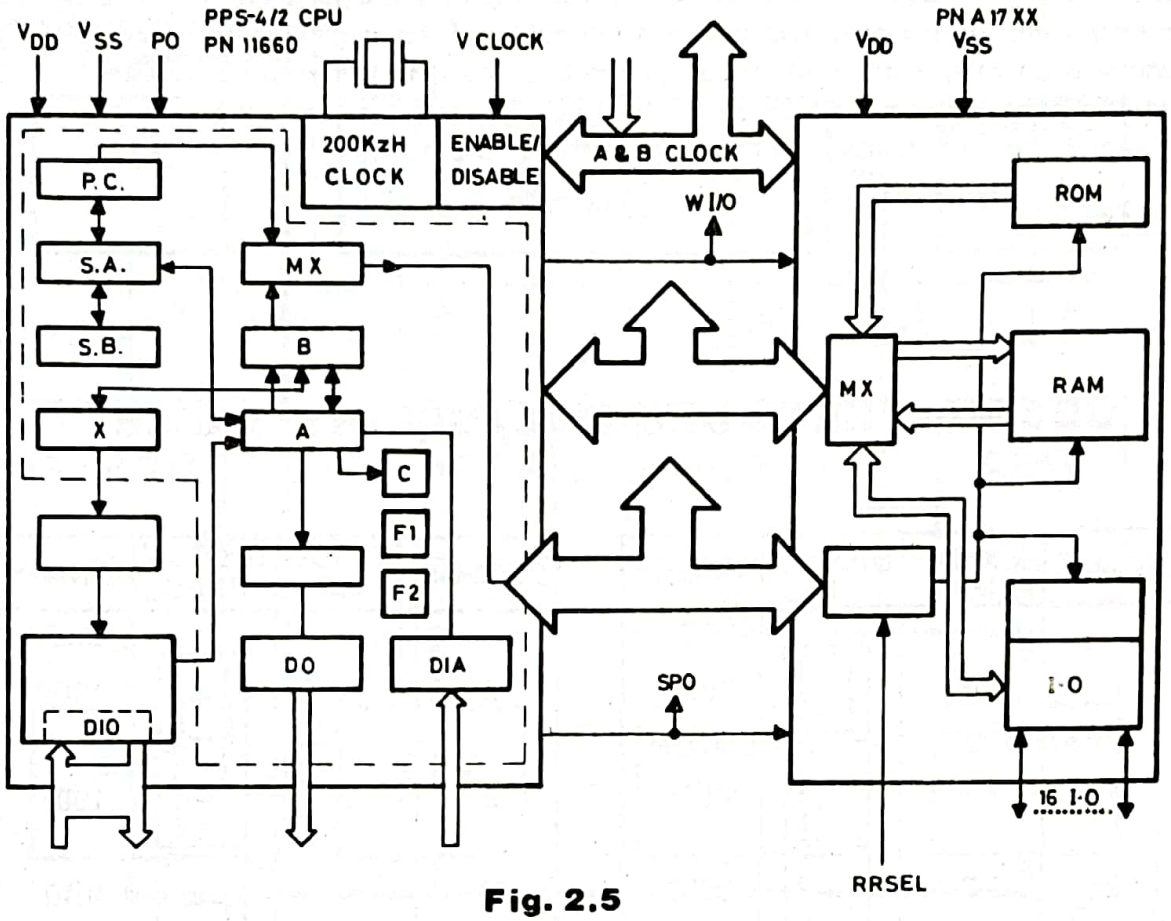

Fig. 2.5

In Fig. 2.5 we can see a simple but real system the layout of which requires only two (2) chips.

The more important registers have been depicted on the CPU chip. "A" is the main working register (accumulator), through which all data from RAM, I/O, DO, DIA, etc., pass and where all types of logical and arithmetical operations are performed. "B" is the register that contains the address of the RAM, which can be read or altered. "P.C." (program counter) is the register that addresses the ROM memory (program). "S.A. and S.B" are registers that enable the program counter (P.C.) contents to be stored, to carry out any sub-routine (situated somewhere else in the program) and come back to the main program, restoring the P.C. contents. "D.O., DIA and DIO" are system inputs and outputs incorporated in the CPU chip.

The second chip contains the ROM, RAM memories and an I/O circuit with 16 inputs/outputs.

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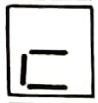
As we can see, this assembly made up of two chips, contains all the basic parts required to control and manipulate data, hence the number of chips is not the significant factor (the system could be of just one), everything depending on the number of functions incorporated in the chip or chips and of course, the maximum capacity of them (ROM memory and RAM memory capacity, number of inputs/outputs, and CPU instruction power) and the time required to carry out a specific instruction or movement; in our case, the movement of a clock taking 5 μsecs.

DECIMAL/HEXADECIMAL/BINARY TABLE

DECIMAL	HEXADE-CIMAL	DISPLAY PRES.	BINARY DCBA
0	0		0000
1	1		0001
2	2		0010
3	3		0011
4	4		0100
5	5		0101
6	6		0110
7	7		0111

DECIMAL	HEXADE-CIMAL	DISPLAY PRES.	BINARY DCBA
8	8		1000
9	9		1001
10	A		1010
11	B		1011
12	C		1100
13	D		1101
14	E		1110
15	F		1111

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2.4 STRUCTURE OF SYSTEM III

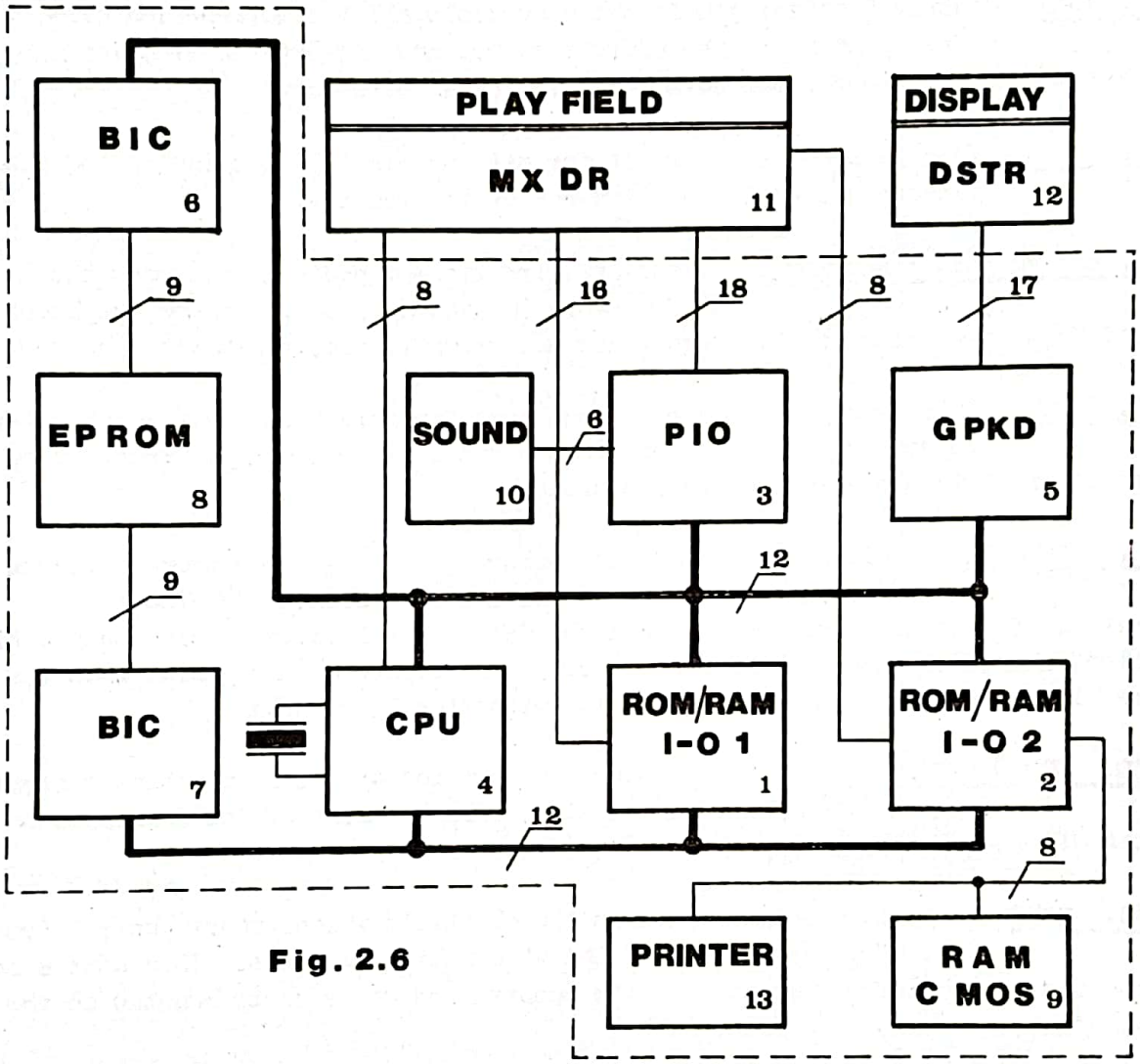

Fig. 2.6

With reference to Fig. 2.6 and following the order of the numbering shown for each chip or unit, we will now briefly define the functions that they carry out.

1. ROM/RAM I-O 1 This chip consists of 3 parts: a) ROM which contains the first 1000 program bytes (words of 8 bits); b) RAM containing the first 128 data bytes (words of 4 bits); c) I/O 16 outputs used as registers for the playfield.

2. ROM/RAM I-O 2 This is a chip the same as (1) but containing: a) ROM with the 2nd 1000 program bytes; b)RAM with the 2nd 128 data bytes; c) I/O with 8 outputs which can be used as registers for the playfield and 8 outputs controlling the RAM CMOS memory and printer.

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3. PIO Circuit of 24 I/O's using all of them as outputs in the following way: 6 as sound control outputs; 10 to control the playfield coils; and 8 to control the playfield registers.

4. CPU Central Processing Unit which controls all the surrounding circuits by means of the addressing bus and the Data/Instruction bus. This CPU is described under paragraph 2.3. (Real Structure).

5. GPKD This is a control circuit for all the displays and indicating registers housed in the lite-box of the machine.

6. and 7. BIC 1 and BIC 2 These are circuits which direct and read the EPROM memory (Gaming program), because the level and form of working of this memory are not directly compatible with the CPU.

8. EPROM This is a program memory that contains only those data which refer to each particular model (256 bytes). This memory is recorded by an internal impulse-produced fusion process.

9. RAM CMOS An ultra low consumption memory ($< 1\ \mu A$) which stocks all the data during the time the machine is switched off from the mains. Its power supply meanwhile comes from a small battery which has sufficient charge to maintain the memory active for more than one year. When the machine is switched on, the battery is automatically recharged.

10. SOUND SYSTEM This is an assembly comprising 4 T T L chips which generate the sounds and control them by means of the 6 outputs on the PIO (see 3 above).

11. MXDR This is a unit mounted on the playfield which, under control from the CPU, selects any of the 40 existing switches. This unit also contains the drivers that control the bumpers and other parts mounted on the playfield.

12. DSTR This unit is controlled by the GPKD and activates all the digits and indicators mounted in the lite box of the machine.

13. PRINTER Used to print out and change data in the memory.

NOTE: The main program is distributed in Chips 1 and 2, and comprises a total of 2000 bytes (8 bits per byte), whereas the game program (contained in PROM) consists of only 256 bytes.

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2.5 PHILOSOPHY OF SYSTEM III

The functional basis of the system is simple and clearly summarised in the following points :

a) The entire functioning of the system is controlled and dictated by the Master Unit.

b) The remaining units are only indicators, or interfaces for these.

c) If the Master Unit and its power supply voltages are correct, there can only exist the possibility of abnormal functioning if the contact read-out information is defective (in which case all the functions will be carried out well, but in response to contacts which are not relevant for each function).

d) In order to carry out a proper analysis of the system, it is advisable to consider all the elements which do not belong to the power supply nor Master Unit as indicators. A display is an output indicator which expresses a determined value; a lamp is an output indicator which represents a state, either lit or unlit; a coil is an output indicator which represents a state, either activated or disactivated; a contact is an input indicator which also expresses a state, either open or closed.

On the basis of these considerations we can establish two classes of possible faults: a fault in the actual functioning (Master Unit) and a fault in the indications (easily found by means of the logic detector or test probe).

In order to carry out repairs "in situ", the most practical and rapid means is to substitute the faulty unit for another in proper working order. This is why we have intended and succeeded in producing with the System III a pinball machine where absolutely each and every one of the units are interchangeable, from model to model; including between single and four player games.

e) In the general diagram (shown below) you can see clearly how the Master Unit controls the rest of the machine via two main ways : lite box control and playboard and cabinet control.

The numbers (N) indicated on this diagram, specify the page number of Section 5 on which each unit is described.

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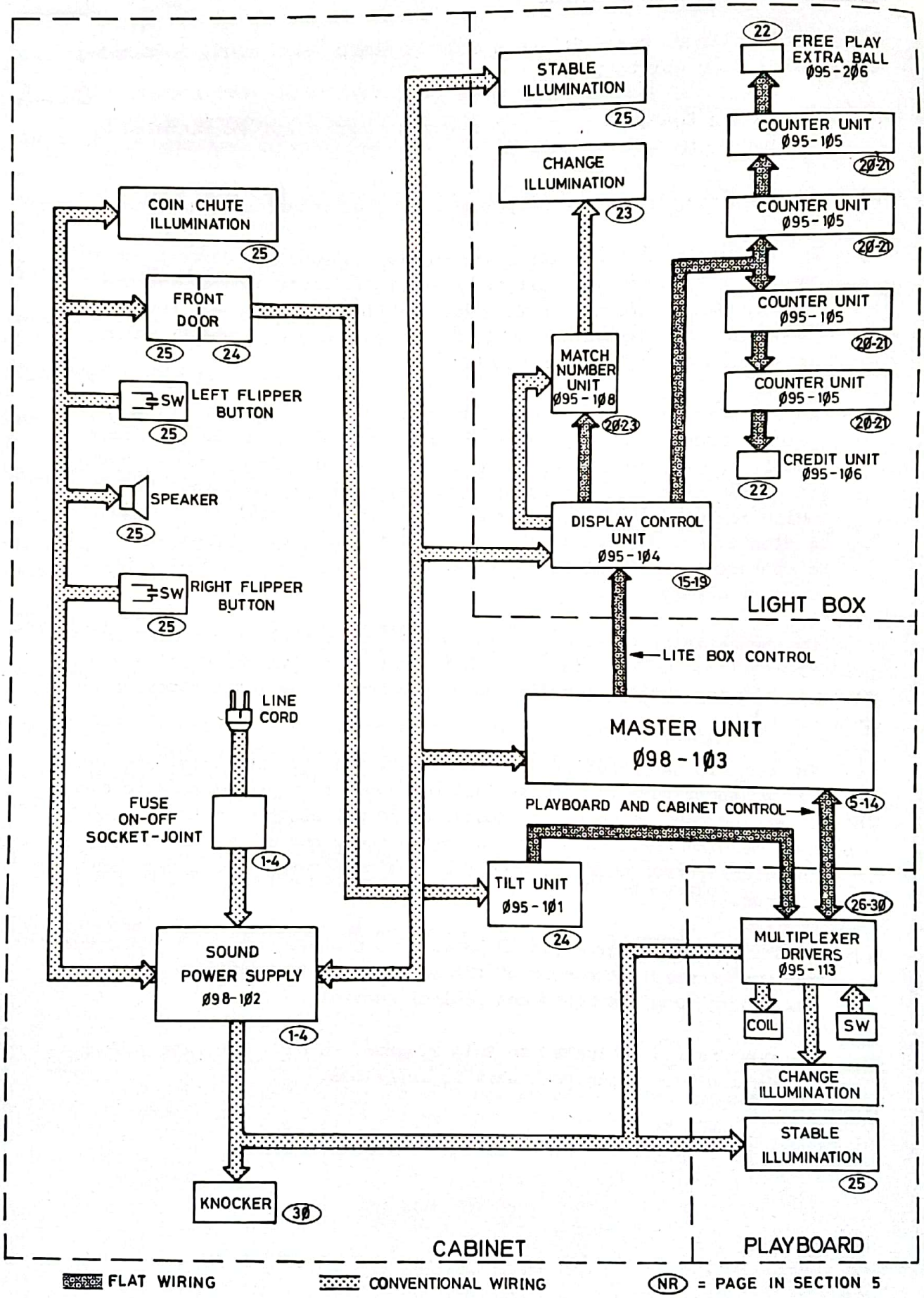
FUNCTIONAL DIAGRAM



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SECTION 3

DESCRIPTION

3-1 GENERAL FUNCTIONS

A normal pinball machine, in the four player version, must offer and offers the following characteristics : coin-slot operation, adjustable tariffs, an indication of the games paid for, four score counters, three or five balls, start button, fault and tilt contacts and indicators, extra ball, free plays obtained from the score (adjustable), match number and flexibility in the system to give any game on the playfield.

The SYSTEM III pinball complies with the above mentioned specification and also offers the following feature :

3-2 SELFCHECK

As soon as the machine is connected (using the switch on the right hand underside of the table), a Self-Check routine starts which covers the electric and electronic systems, indicating any fault and identifying the same; if this routine detects a "major" fault (e.g. a short circuit in the coils, driver or I/O RAM failure, etc.), it decides not to continue operating but indicates the fault. Should a "minor" fault be detected (e.g. a coil out, I/O open circuit, short in I/O lamp, etc.), the system will indicate the fault and automatically continue carrying out its function.

The Self-Check routine consists of 6 steps and the results are shown on the display corresponding to Player Nº 2.

1. Lite Box Display and Indicators
   All displays and indicators mounted in the lite-box, will be lit up in sequence in all their combinations. When completed, you will see the indication Ø Ø Ø.

2. RAM Memory
   This function inspects byte by byte all the RAM (shared between the Chips 1 and 2). If everything is in order, you will see the indication 9 Ø Ø.

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If it detects a fault in any of the 256 bytes, it will indicate such a fault in the two digits following the number 9, e.g.: byte 87 is at fault - the system will indicate 9.8.7., in accordance with the hexadecimal code. (Note 1).

3. PIO (Chip controlling Sound, Coil & General Indicators in the Playfield)

If everything is in order, this will indicate 8.Ø.Ø. If there is a faulty output, it will indicate X.X.X., specifying via the X which is the output concerned, and what is the actual fault.

4. ROM I/O

Two chips incorporating the ROM memory, RAM CMOS control outputs and playfield lamp control outputs. This function analyses one by one all the inputs and outputs. If everything is in order, it will indicate 2.4. . If the fault lies in Chip 1, it will indicate 1.X.X., and if the fault is to be found in Chip 2, 2.X.X. The last two digits indicate the output which is at fault, and the reason why.

5. Sound, Coil Drivers and Coils

This check is made by reading the consumption at the power play supply source, and will indicate, as a "major" fault, the lack of tension, a short circuit in the driver and a short circuit in the coil; and as a "minor" fault, those channels which do not provoke any consumption of the above mentioned supply source (sound, unused channels and drivers or disconnected or cut-off coils). As always the channel and problem will be indicated.

6. RAM CMOS

This function individually checks the 1024 bits in the memory. If all is well, it will indicate 5.Ø.Ø. If a fault is discovered, it will indicate the byte which is at fault.

If it detects a fault, and when repeating the Self-Check routine it does not indicate the same fault code, the problem is to be found in the stabilization or faulty power supply filter, and the alternative component is the cause of the different readings.

Note 1: If the fault is indicated as 9.7.F or less, this means that the A2361 chip is broken; in all other cases, the problem is to be found in the A2362 chip.

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SELFCHECK TABLE

ALL INDICATIONS ARE IN THE SECOND PLAYER DISPLAY

STEP	FUNCTION	DISPLAY	OBSERVATIONS
1	TEST DISPLAY	Ø Ø Ø	END OF TEST DISPLAY
2	RAM MEMORY	9 X X	FAULT DETECTED. THE LAST TWO DIGITS INDICATE POSITION AT FAULT. (1)
2	RAM MEMORY	9 Ø Ø	END OF TEST. RAM (O.K.)
3	PIO	X X X	1ST DIGIT INDICATES GROUP 3-4-5-6-7-8 2ND DIGIT INDICATES THE DEFECTIVE BIT * (1) 3ND DIGIT INDICATES DEFECTIVE CONFIGURATION
3	PIO	8 Ø Ø	END OF TEST. PIO (O.K.)
4	ROM I/O	1 7 X	SHORT IN OUTPUT X AT -12V (CHIP-1)
4	ROM I/O	1 4 X	SHORT IN OUTPUT X AT +5V (CHIP-1) *
4	ROM I/O	2 7 X	SHORT IN OUTPUT X AT -12V (CHIP-2)
4	ROM I/O	2 4 X	SHORT IN OUTPUT X AT +5V (CHIP-2) *
4	ROM I/O	2 4	END OF TEST. ROM (O.K.) → SHORT TONE ←
5	PW. PLAY VOLTAGE	2 4 6	VOLTAGE FAULT (POWER PLAY) (1)
5	DRIVER	2 4 5	SHORT IN DRIVER (1)
5	COIL	X 4 7	COIL X OPEN. / TEST SOUND (X≤5)
5	COIL	X 4 4	SHORT IN COIL X (1)
5	DR/CL	3 Ø Ø	END OF TEST. DR/CL (O.K.) NO MAJOR FAULTS DETECTED
6	RAM CMOS	8 X X	FAULT DETECTED. THE LAST TWO DIGITS INDICATE THE DEFECTIVE WORD (1)
6	RAM CMOS	5 Ø Ø	END OF TEST. CMOS (O.K.)

*IF THE OUTPUT IS OPEN CIRCUITED IT WILL INDICATE +5

(1) MAJOR FAULTS

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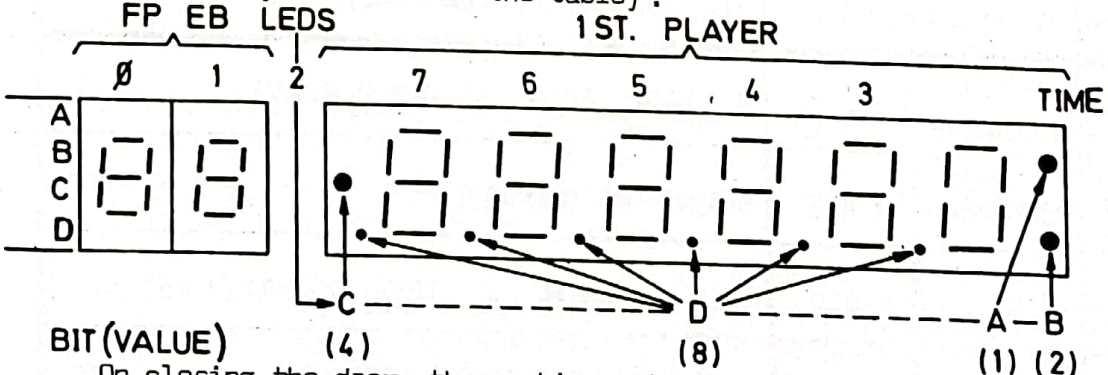
3-3 REPRESENTATION AREAS

Areas of Representation for the totalizers and RAM memory registers: As stated before, the SYSTEM III accumulates a quantity of information, up to now unknown in the field of pinball machines. All this information is represented on the displays as follows: whilst the door is shut, the display always represents that shown in Area 4 which corresponds to the actual play data, and when you reach Game Over, it will alternatively flash data on the last score and last handicap (highest score).

On opening the door, the start button will stop working as such and will serve to change the area representation on the displays. There are 16 representation areas on the RAM (see page 3-5). In order to advance from one area to the next, you need only press the button once for each advance of area representation. Whilst the button is pressed down, all the lite box displays will indicate the number of the area which is going to be represented next. Then on releasing the button, the displays will show the data corresponding to each new area. If we press the button just once (starting from area 4), it will stay in area 5 representation, but this will have been inverted; i.e. the information that was previously in the upper displays, will now be shown in the lower displays and vice-versa, (we will understand the advantages of this in the section on ADJUSTMENT).

In the representation area 6, we can see the state of the playfield contacts, which are indicated in the displays for Free Plays, Extra Ball and 1st Player (see values in the table).



On closing the door, the machine automatically stays ready for play, returning to the preselected area if the door were to be opened again before pressing the start button. When started, the area selected stays at 4.

As can be appreciated, the system provides for a total read-out of the RAM memory. This is why some of the data might be of little interest, without full knowledge of the system.

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REPRESENTATION TABLE

DISPLAY ON	REPRESENTATION AREAS Ø-4-8-U	REPRESENTATION AREAS 2-6-C-E
X X	WORKING REGISTERS	CREDIT LIMIT X | X LIMIT = X9
X X X X X Ø	WORKING REGISTERS	MODEL OF GAME *
X X X X X Ø	WORKING REGISTERS	SERIAL NUMBER *
X X X X X Ø	LAST PRINTER CODE	TIME IN PLAY (XXXXXX)
X X X X X Ø	PLAYBOARD REGISTER STATE	TIME GAME OVER(XXXXXX)
X X	PLAYBOARD REGISTER STATE	SECONDS TIMER (CENTESIMAL)
X X	FREE PLAY (COUNTER) X | X EXTRA BALL (COUNTER)	REPLAY PER XXØ.ØØØ
X X X X X Ø	PLAYER Nº1 (COUNTER)	HANDICAP PLAYER Nº 1
X X X X X Ø	PLAYER Nº2 (COUNTER)	HANDICAP PLAYER Nº 2
X X X X X Ø	PLAYER Nº3 (COUNTER)	HANDICAP PLAYER Nº 3
X X X X X Ø	PLAYER Nº4 (COUNTER)	HANDICAP PLAYER Nº 4
X X	CREDIT (COUNTER)	REPLAY PER XXØØØØ
X X	EXTRA BALL PER XXØ.ØØØ	1 ST COIN REJECTOR(ADJ) X | X 2ND COIN REJECTOR(ADJ.)
X X X X X Ø	TOTAL 1 ST COIN REJECTOR	TOTAL EXTRA BALL
X X X X X Ø	TOTAL 2ND COIN REJECTOR	TOTAL FREE PLAY
X X X X X Ø	TOTAL 3RD COIN REJECTOR	TOTAL PLAY SERVICING
X X X X X Ø	DATE OF LAST PRINT-OUT	TOTAL PLAY METER
X X	FORM OF PLAY *	3RD COIN REJECTOR(ADJ) X | X MODE OF PLAY(ADJ)
X X	PLAYBOARD CONTACTS READ	PLAYBOARD CONTACTS STATE
X X X X X Ø	PLAYBOARD CONTACTS READ	PLAYBOARD CONTACTS STATE
X X X X X Ø	RESERVE TOTALIZER 1 *	RESERVE TOTALIZER 3*
X X X X X Ø	RESERVE TOTALIZER 2 *	RESERVE TOTALIZER 4*
X X X X X Ø	PLAYBOARD CONT. DEBOUNCE	PRESET CONTACTS TIME
X X	PLAYBOARD CONT. DEBOUNCE	PRESET CONTACTS TIME

*SPECIAL GAME SERVICE

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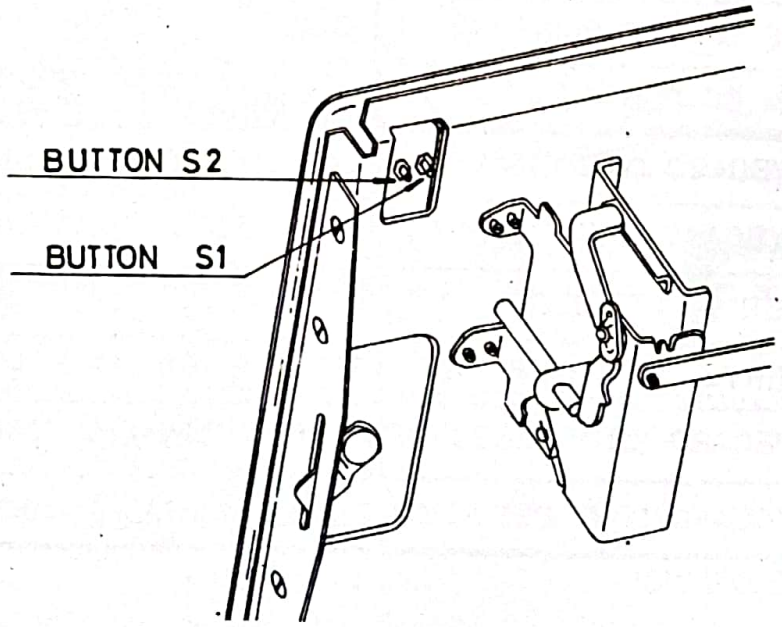
3-4 HANDICAP

During the time that the machine is at Game Over, the Handicap of each player will be flashed on the displays. It will also be displayed whilst the start button is held down (assuming that the door is closed). The machine leaves the factory with a Handicap for each player of 1.000.000. This value is altered as soon as it is beaten. When the new Handicap exceeds 2.000.000, the respective handicap register stays at 1.000.000, and in this way the machine incorporates an automatic resetting device should the handicap become excessively high.

3-5 ADJUSTMENT

There are three RAM memory areas where you will find the various system adjustments.

To gain access to alter any of these, simply select the relevant representation area on the credit displays (with the door open and by pressing the start button). When set in this position, press the buttons S1 or S2 which are mounted on the inside of the door, in order to change the left or right hand digits, thereby altering the reading to the desired value. Once the adjustments have been set as required, start the machine in the normal way (with the door shut), so that the new values will have been recorded in the RAM CMOS memory.



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GENERAL ADJUSTMENT TABLE

YOU CAN SEE THIS NUMBER PRESSING THE START BUTTON (IN ALL DISPLAYS)

AREA	CREDIT DISPLAY	ADJUSTMENT FUNCTION		
6	XX	REPLAY PER XX□□□□ POINTS		
7	XX	REPLAY PER XX□□□□ POINTS		
9	XX	EXTRA BALL PER XX□□□□ POINTS		
C	X■	3RD. COIN REJECTOR (X=PLAYS PER COIN)		
	■X	MODE OF PLAY (X = A + B + C)		
		A=	Ø	EXTRA BALL NOT REPETITIVE
			1	EXTRA BALL REPETITIVE
			2	EXTRA BALL ACCUMULATIVE
		B=	Ø	FREE PLAY NOT REPETITIVE
			4	FREE PLAY REPETITIVE
		C=	Ø	5 BALLS PER PLAY
			8	3 BALLS PER PLAY
J	X■	1ST COIN REJECTOR (X = 8 + D + E)		
		D=	Ø	1 PLAY
			1	2 PLAYS
			2	3 PLAYS
			3	4 PLAYS
		E=	Ø	2 COINS
			4	1 COIN
	■X	2ND COIN REJECTOR (X = D + G)		
		D=	SEE REJECTOR 1	
		G=	Ø	NORMAL PRICE
			8	PREMIUM PRICE *

* 1 EXTRA PLAY WITH 2ND PAYMENT (min. 1 play) WITHOUT PRESSING THE START BUTTON
(THIS STATE AFFECTS ALL 3 COIN REJECTORS)

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3-6 LOGIC DETECTOR

Ø94-629

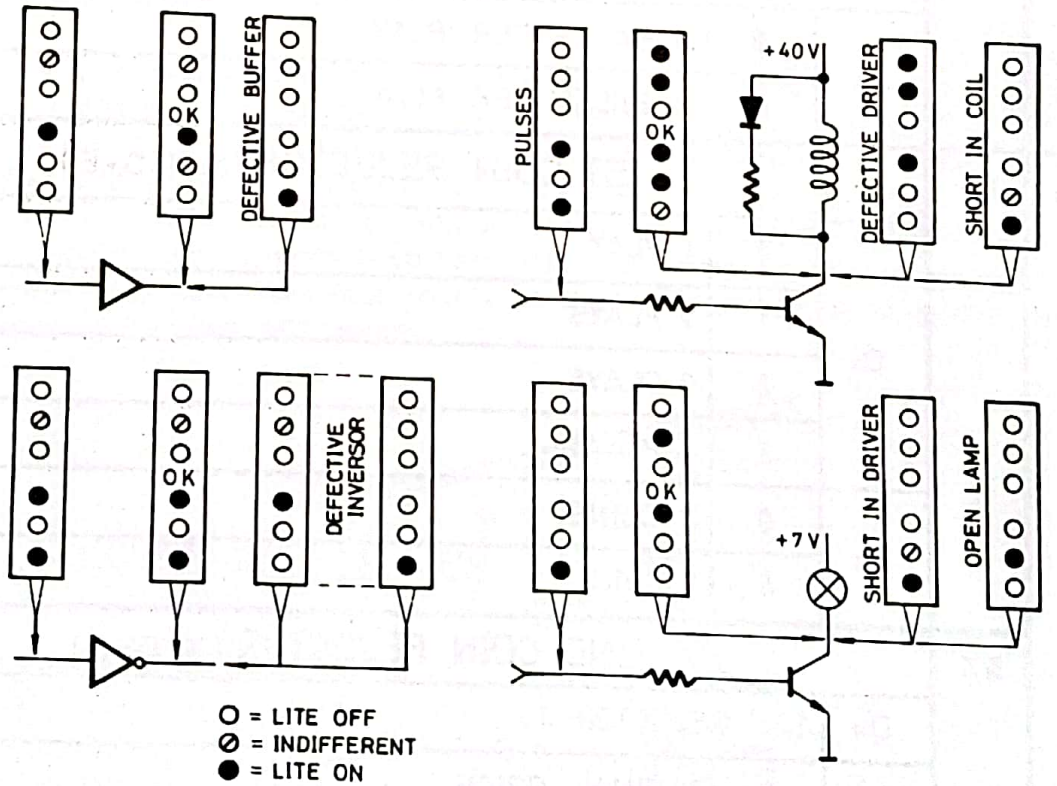
The Test Probe 094-629 is a pulse detector and level indicator which has been designed specially for servicing SYSTEM III.

It contains all the necessary indications for carrying out measurements on any unit and point of the system. This probe 094-629 if used correctly, is the only pocket instrument which makes it possible to find any fault on the system.

The probe cannot take measurements from the mains, for which reason it is recommendable that the service engineer carries a standard multimeter, especially when installing the machine at an unfamiliar site.

On the enclosed table we have shown the indications given by the test probe, with some types of pulses.

By way of an example, below we are showing the measurements taken on some practical circuits.



Logically these examples are only a sample and the indications in all cases are very easy to interpret. The duty cycle of a signal is in proportion to the brilliance of the LED, denominated +7.

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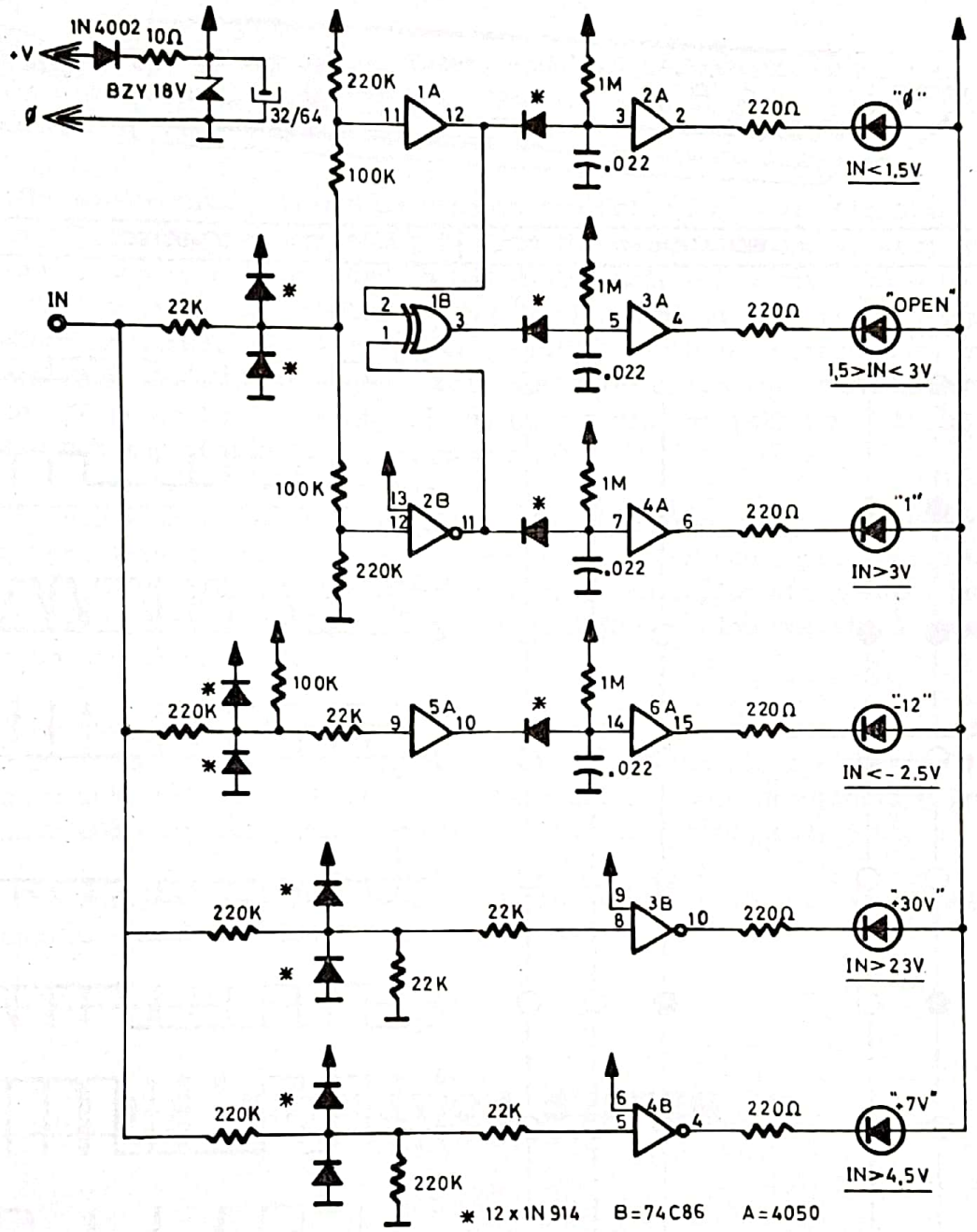
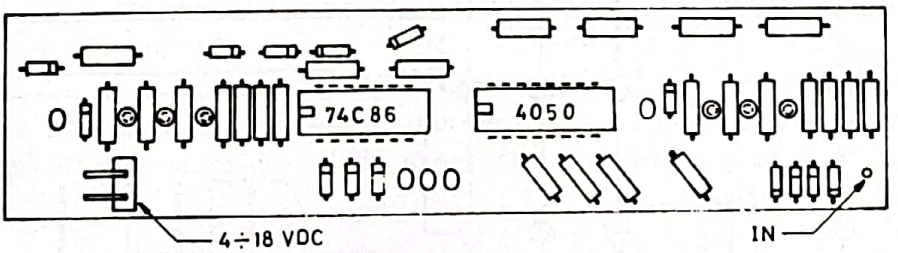
LOGIC DETECTOR DIAGRAM



BOARD ASSEMBLY



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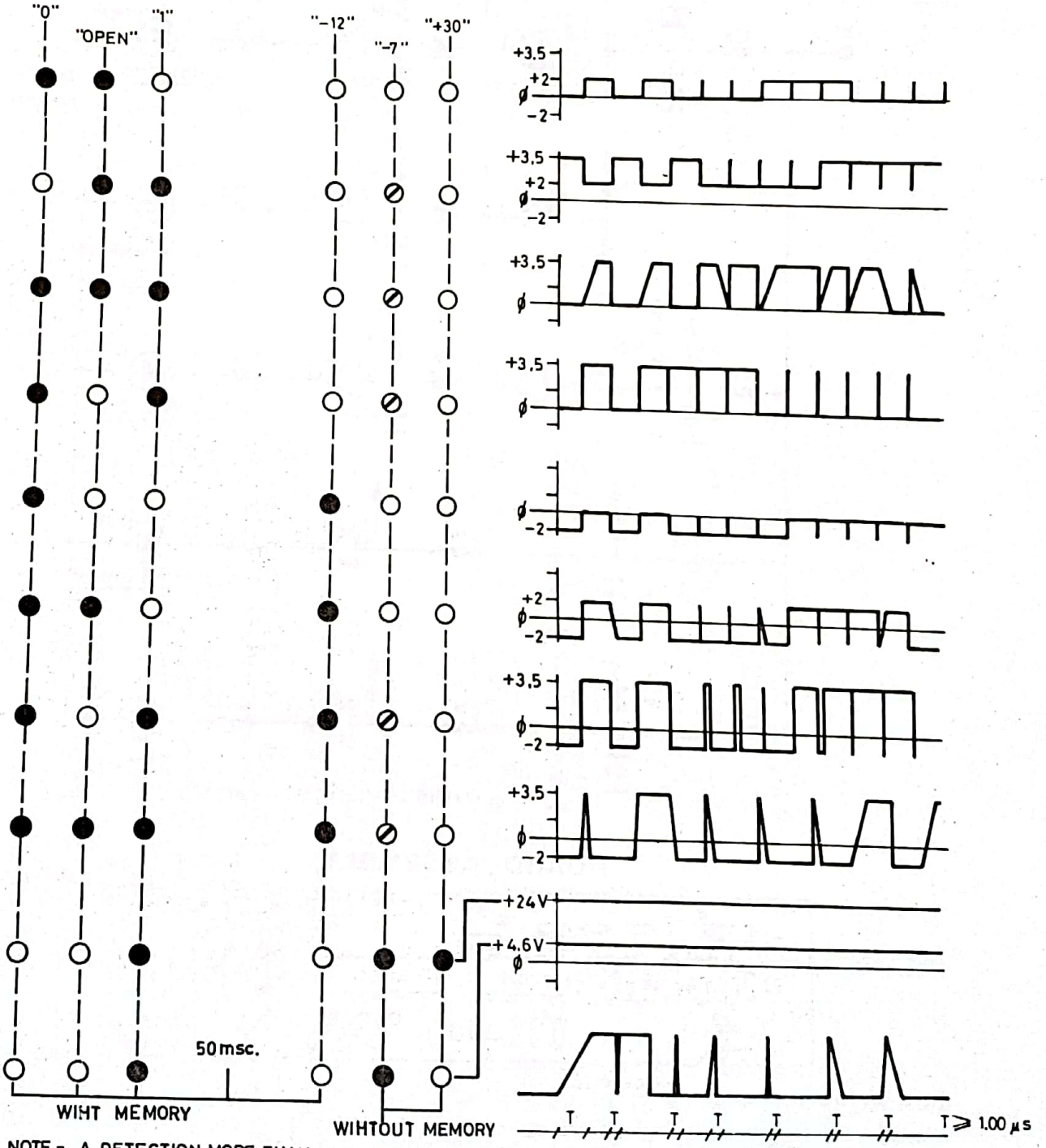
LOGIC DETECTOR TABLE

(LEVEL INDICATOR – PULSE DETECTOR)

INDICATION	SIGNAL DETECTED



NOTE:- A DETECTION MORE THAN 1.00 µs. WILL PROMOTE A FLASH OF 50m.sec.(INDICATOR "X")
INPUT IMPEDANCE=100K TO ϕV ⊘ DUTYCICLE INDICATION

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3-7 MINIPRINTER

Correct use of our Mini-printer, model 2056A, constitutes a really valuable advantage to gain the most from the special characteristics incorporated in the SYSTEM III.

The mini-printer should be used in the following way: firstly, switch off the machine or unplug it from the mains. Secondly, plug in the printer to the socket provided in the Master Unit - connector MD - to be found in the lite box. Replug in the machine and wait for it to finish the Self-Check routine. Check that the resettable date and printer number registers have absorbed the new values correctly; press the start button; switch off or unplug the machine; unplug the printer (all the data is printed out and stored in the printer memory).

If you wish to use the printer merely to obtain data, but without it being necessary to reset any of the registers, then you should not press the start button, but switch off the machine and unplug the printer instead. The data is now in the printer, and the machine registers have not suffered any alteration.

The modifications that the printer creates over the registers and totalizers in the machine are programmed in advance within the printer itself and come into effect when you press the start button, and selecting only the date and coin collection number (if this is the object).

The working printer mode and time are explained in the Master Unit explanation (next Section).

3-8 SIMULATION SYSTEM III

The checking Simulator 094-630 makes it possible to check, analyse and simulate all components on our System III electronic pinball. It has an internal capacity to simulate and control 16 games which may be increased by external blocks of 16.

Also it contains the necessary connections to enable the substitution of all parts of the machine and to start functioning any unit of the laboratory.

The Simulator 094-630 is supplied with its own full technical manual.

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SECTION 4

MAINTENANCE

4.1 GENERAL CONDITIONS: The SYSTEM III pinball machines require regular periodic inspection of the conventional electro-mechanical parts: a) cleaning in general, particularly of the playfield; b) replacement of the rubber rings; c) inspection of the coil stops, plungers, springs, brackets and bumper fittings; d) illumination and indication lamps; e) revision of contacts, running check in presentation area (see paragraph 4.4).

The actual electronic system does not require routine maintenance, but the service engineers should comply with the following points :

DO NOT CARRY OUT CONNEXIONS, DISCONNEXIONS OR SOLDERING on any part whilst the machine is switched on.

USE THE SELF-CHECK ROUTINE to trace any type of fault that might occur and to repair it.

TO TAKE MEASUREMENTS use a multimeter and our Pulse and Logic Detector (test probe) Ref. 094-629, or its equivalent.

FOR COMPLETE REVISION in a laboratory, the Simulator 096-630 is the only equipment capable of simulating all the functions of the SYSTEM III.

PROBLEMS IN THE POWER SUPPLY: Pull out the PB and PC connector from the supply circuit (with the machine off) and repair the fault, plugging in the connector again (still with the machine off) once you have checked that all voltages are correct.

If maintenance is carried out on the basis of the above hints, you can be sure that the machine will have a virtually limitless life duration.

4.2 COILS: The Self-Check routine detects the two possible faults that could occur in a coil, namely: short or open circuit. If a short circuit is indicated (X.4.4), we suggest you check the relevant diode, connections and mounting (as this fault by itself is almost impossible, and the machine would have detected excess consumption, making the thermal circuit breaker jump). If an open circuit is indicated (X.4.7), the driver and its connections should be checked with the help of the pulse and logic detector (094-629 Test probe), because the Self-Check routine has detected zero consumption.

When replacing a part it is important to ensure correct polarity and proper soldering.

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4.3 LAMPS: During the Self-Check routine, a test is made on all outputs (peripherals of the processor) controlling the indicator lamps. This enables, when there is no indication of a fault, to see whether the problem lies in the lamp if this does not lite up, or in the driver if the lamp never goes out.

When replacing a driver or an indicator lamp, a quick check of the relevant connector is recommended.

During the Self-Check routine, all the lamps and indicators in the system will be lit up.

4.4 CONTACTS: All types of faults in the contacts (including faulty adjustment) will be shown up in the memory area E; in this area, on the displays corresponding to "free play", "extra ball" and "first player", a permanent and simultaneous reading is obtained of all the contacts in the playfield. Each contact is represented by a digit and a value defined in the corresponding game Service Manual. Each digit can represent the condition of four contacts simultaneously, the value of these being (if they are closed) equal to 1, 2, 4 and 8 respectively; the digit therefore indicates the sum corresponding to the contacts closed.

The following example is given to clarify this point. Four contacts, which we shall call 4A, 4B, 4C and 4D are presented in position 4 (see Fig. 4.1); if 4A and 4B are closed, whilst 4C and 4D are open, the digit will indicate 3; then if 4A is opened, it will indicate 2, and if now 4C is closed, it will show 6. We can thus see that the reading is very straightforward and that the position and value of each contact is implied in its reference number; the first number indicating its position in the display and the second its value. We recommend that the service engineer should familiarize himself with the hexadecimal code and its presentation in the display (see table).

The contacts related to general operations, (start, coin microswitches, tilt fault and selectors 1 and 2) are represented on the indicators corresponding to the Match Number and Game State (Tilt, Game Over or Ball in Play lamps) and their values are as follows :

FAULT	COIN 1	COIN 2	COIN 3	TILT	START	SELECT 1	SELECT 2	SWITCH
1	2	4	8	1	2	4	8	VALUE
Shown in Game State U or E (Tilt, G.O., Ball in Play)				Shown in Match Number U or E				READ IN

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REPRESENT. CODE	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LAMP LIT	1	2	3	4	5	G	G	G	1-T	2-T	3-T	4-T	5-T	G-T	G-T	G-T
	T = Tilt G = Game Over Nº = Ball In Play															

Note: The contact for the door and tilt is the same one, and therefore the door has to be open whilst inspecting the areas (contact closed), the reading of this will always be activated.

The playfield contacts are represented in the mentioned area E, and in the relevant code the position (digit) is shown quite implicitly, as well as the value for that position. The number indicates the position and the letter shows the value (A = 1, B = 2, C = 4 and D = 8).

POSITION

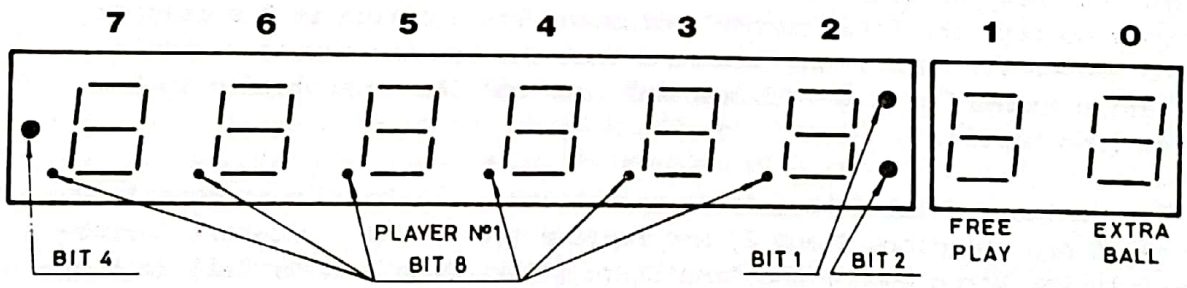

Fig. 4·1

For example: Contact 5B will be represented on indicator 5 (thousands unit for the 1st player) by value 2 (if it is closed). If various contacts are closed at the same position, the value shown would be the sum of the value of each of those contacts.

4.5 GENERAL DIAGRAM: The following diagram corresponds to the general schematic of the System III pinball where for greater clarity we have represented in block form the various units which will be described in Chapter 5.

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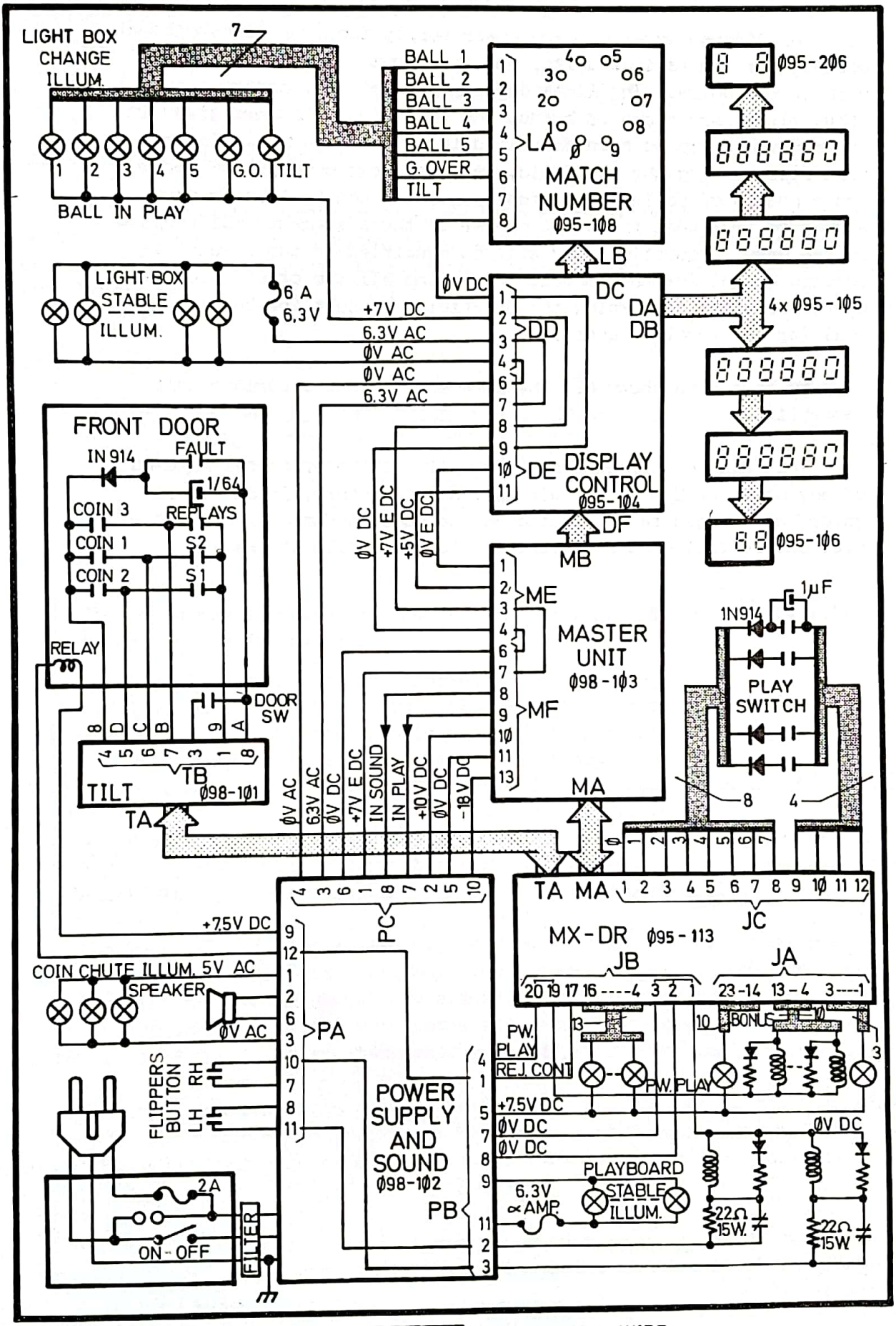
MACHINE DIAGRAM



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The diagram shows all the power supply tensions (conventional wiring) for the various units, and the input and output pins for each of the units. The lines corresponding to the control signals (flat wire), are shown as buses, and their functions are given in the section where we have described the relevant units. In the part representing the playfield, we have shown a couple of lamps and a couple of coils, separated by points, and by this we have wished to show that the exact number of these elements will depend on the game in question, and will be specified in the respective Service Manual for each model. Regarding all the other specific characteristics concerning the playfield, consult the Service Manual for the model in question.

We have also shown all the references for the various unit assemblies.

This diagram corresponds faithfully to the practical make-up of any model of System III pinball, and therefore, it can be regarded as the general schematic, to be used in the analysis, studies and control of the current and future models of games.

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SECTION 5

MODULES

5.1 POWER SUPPLY AND SOUND

The power supply board is equipped with a transformer primary with the necessary terminals to allow the machine to work correctly at any mains voltage. The relevant terminal position for 12Ø volts, covers a range from 9Ø to 18Ø volts, and the 22Ø volt position covers from 18Ø to 312 v.

135 ÷ 18Ø	122 ÷ 162	1Ø8 ÷ 144	9Ø ÷ 12Ø	RANGE	
15Ø	135	12Ø	1ØØ	12Ø	
26Ø	24Ø	22Ø	2ØØ		22Ø
234 ÷ 312	216 – 288	198 – 264	18Ø ÷ 24Ø	RANGE	

The secondary positions in the transformer supply the necessary voltages to obtain the following :

5 v. AC	Lamps for lighting up the coin rejectors
6.3 v. AC	Stable illumination on the playfield and lite box
+ 7.5 v. DC	Change illumination on the playfield and rejector coil
+ 7 v. DC (E)	Stabilized display - lite box
+ 10 v. DC	(with the Master Unit ON) To obtain 5 v. DC stabilized current for the electronic logic
- 18 v. DC	(with the Master Unit ON) To obtain -12 v. DC stabilized current for the MOS circuits
Power Play	(adjustable) To feed the playboard coils

The Power Play is controlled by the K relay which will cut this power when no "In Play" signal is received. The K contact works in parallel with a 39 ohm. resistor which allows the processor to determine the state of the coils and drivers during the Self-Check routine. This power play is protected by a 3A thermal circuit-breaker with adjustment on the lower side.

The Sound power unit is also to be found in this assembly, and comprises a TIP 132 transistor and a series damper composed of 3 resistors, by means of which the sound level can be adjusted to Maximum (Mx.), Medium (Md.), or Minimum (Mn.).

There is also a series of interconnected pins which allow a better distribution of the cable harness, individualizing the connectors of the Cabinet, Playfield and Lite-box.

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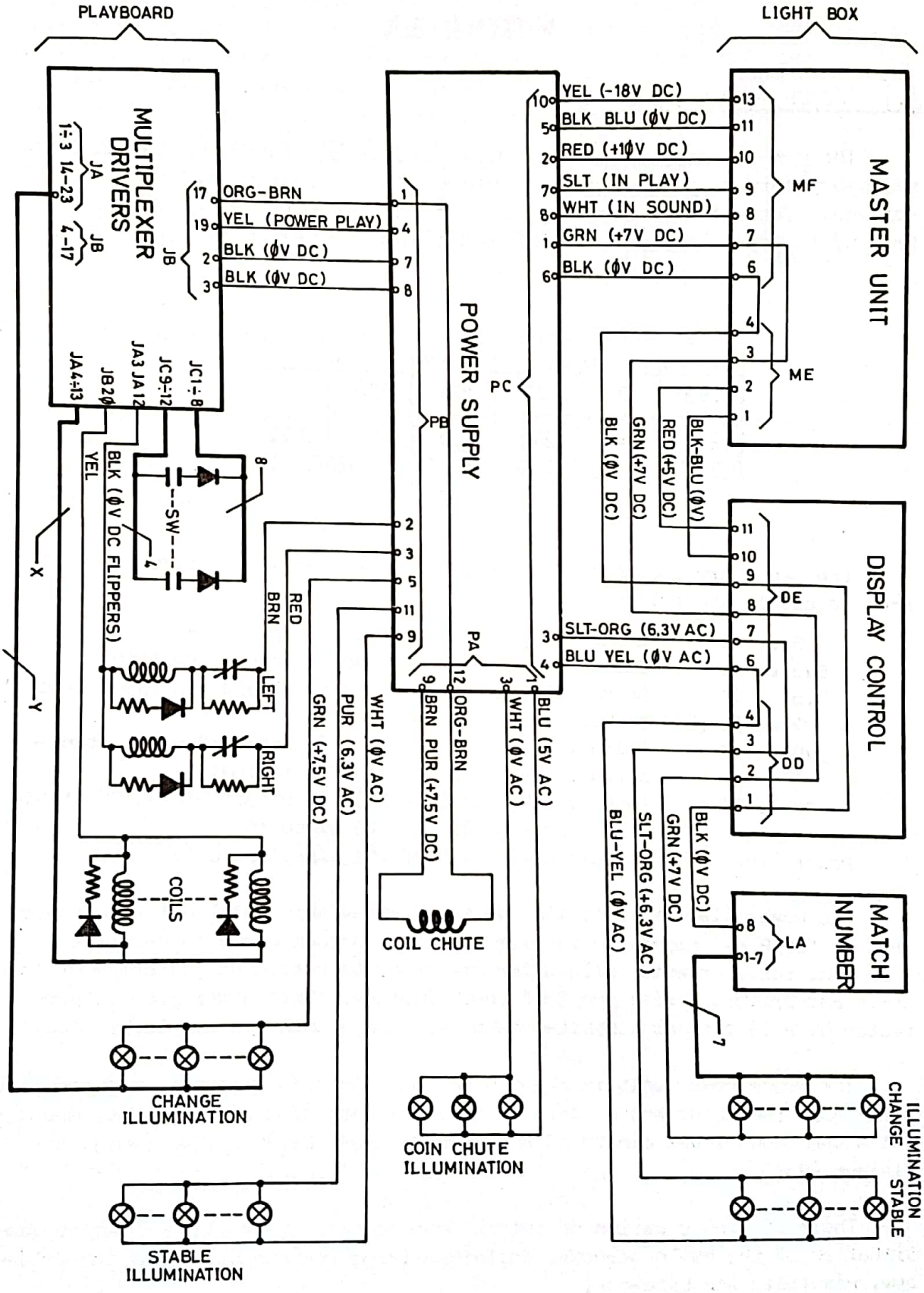
POWER DIAGRAM



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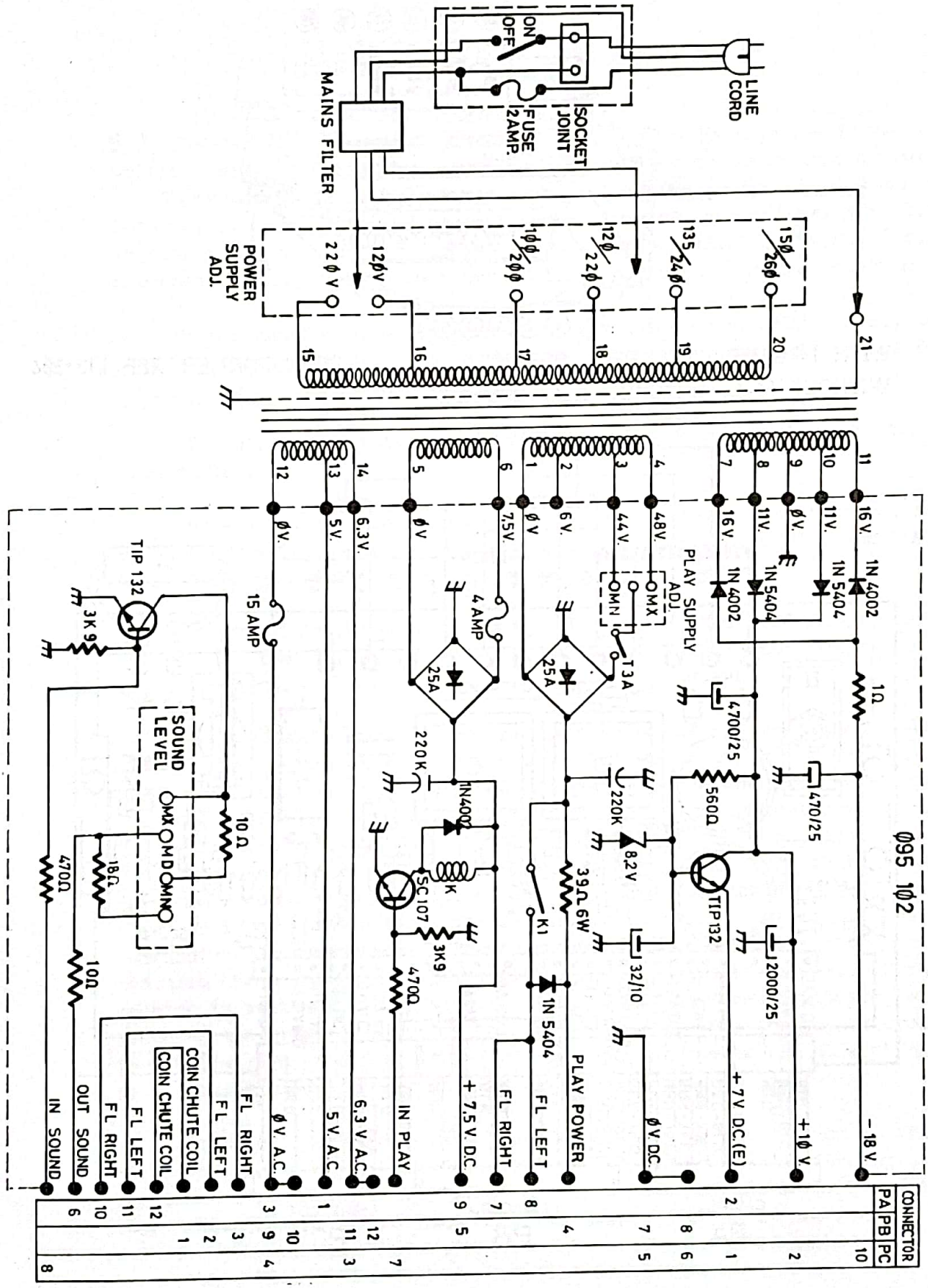
POWER SUPPLY AND SOUND



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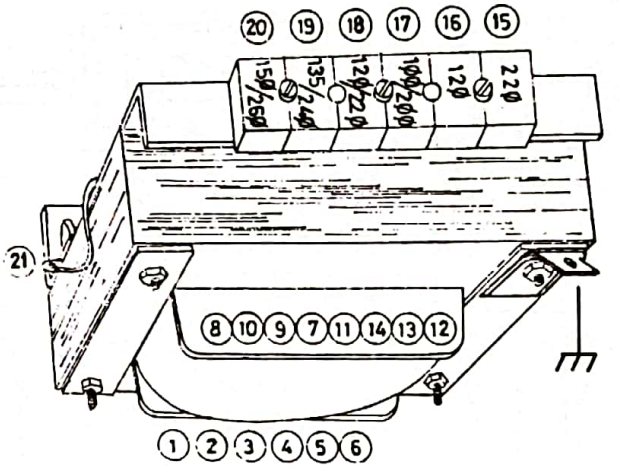
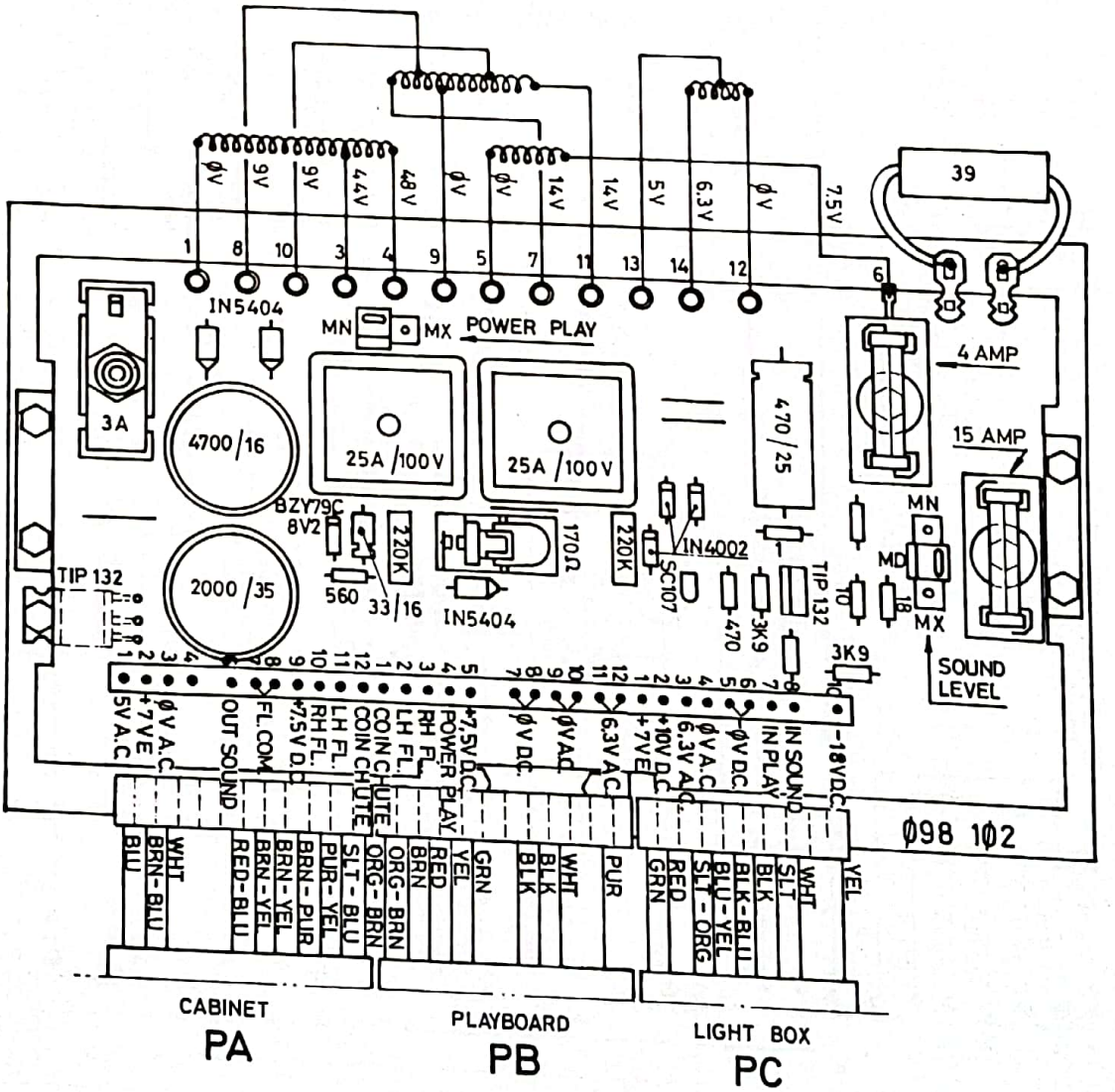
POWER SUPPLY AND SOUND



WITH MTG. BRACKET REF. Ø98-1Ø2
WITHOUT MTG. BRACKET REF. Ø95-1Ø2

TRANSFORMER REF. Ø13-3Ø4



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MASTER UNIT

5.2 The Master Unit needs a working tension of + 10 v. and - 18 v. These voltages are stabilized by the circuit LM 327, which controls a driver MC 140 (output - 12 v. 500 mA max.) and a TIP 3055 (output 5 v. 4 amp max). Both outputs are protected against short circuits, automatically restricting the maximum current to 500 mA and 4 amp respectively, thereby avoiding any destruction of the output transistors should any short circuit occur.

On the tension of + 5 v. and using the union of two F32 diodes, we obtain 6,4 v. which are used to recharge the battery which feeds the RAM CMOS memory HM 6.508-9 and its auxiliary circuits.

If you remove a battery, you will lose the data contained in the RAM CMOS memory.

The - 12 v. tension is required, along with the + 5 v. tension, in order to work the N-MOS chips existing on the board (CPU, PIO, ROM RAM/I-O, GPKD, BICS and EPROM).

All the other chips on the board (TTL and Buffer CMOS 4050), as well as those in the Display Control unit and Multiplexer Driver, use only the + 5 v. tension.

The RAM CMOS memory controlled via the O-6 outputs on RAM-ROM/I-O 1 (A 2361), and after carrying out all the Self-Check routines, delivers its contents to the working memory RAM (contained in chips A 2361 and A 2362). Then the entire contents of the working memory RAM is again loaded on to the CMOS each time that the machine is at the start position or whenever a ball is introduced into the Ball Return Kicker hole. This means that the RAM CMOS can hold all the definitive data and recover this after a power cut. As a result of this feature, it is possible to control the totalizers, adjustments and other registers in the machine (all contained in the memory), and also check their functioning without suffering alterations. If the machine is switched off after carrying out all the necessary tests, without reaching the start position or ball return state, then the data stored in the CMOS will be the same as before carrying out the tests; none of the test alterations will have been memorized.

Whilst extracting the data from RAM CMOS, this information is transferred to the memory of the "Printer" if this is connected, feeding the working memory RAM with the serial number of the printer in use, and this is then passed on to the RAM CMOS once the start position is reached.

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Once the Self-Check routine has been completed, the main program begins and the machine is ready for normal functioning.

In order to control the indicators in the lite box, a GPKD is used as a peripheral element (display controller), to which all the data contained in the area of the memory selected is transferred at the rate of 10 times per second; if the front door is closed, the area selection has no effect and the transfer area will be " 4" (play area). By transferring the data at the rate of 10 c/sec., the displays are subject to a smooth but attractive fluctuation.

The GPKD feeds the information to the display control unit in two groups of data, each one of them formed by 16 displays or other types of indicator. The column selection is carried out by means of 8 Strobe lines and one group selection.

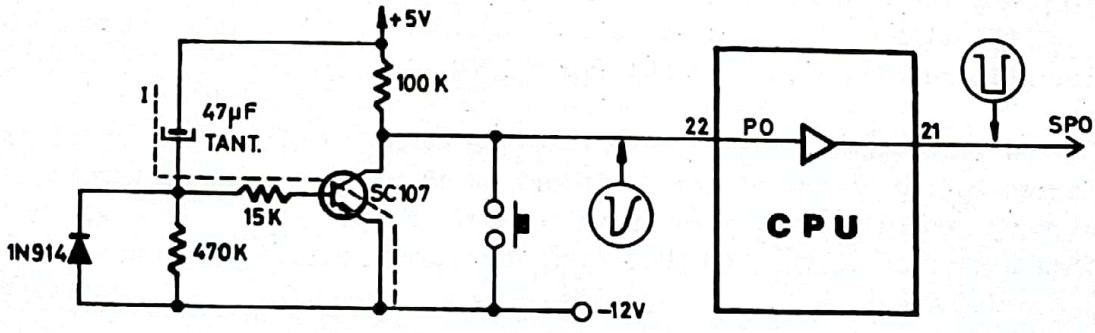
Control of the playboard elements is carried out by means of the PIO peripheral (programable input-output) and the 16 outputs contained in the ROM-RAM/I-O 2 (A 2362).

The PIO has 24 outputs; numbers 0 to 5 control the sound circuit, composed of three gates, an oscillator and a TTL counter and mounted on the Master Unit; output Nº 6 controls the Knocker, Nº 7 the Ball Return driver; outputs 8 to 15 are planned to control other electrical elements on the playboard, and outputs 16 to 23 are used to lite up or switch off the playboard indicators (8).

The 16 outputs on the I-O 2 (A 2362) are also planned to control the lites on the playboard.

The I-O 1 (A 2361) is also equipped with 16 inputs-outputs, of which six are used to control the memory RAM CMOS and the Printer whilst the remaining ten are also available to control elements on the playfield. Therefore there is a maximum of 8 + 8 + 16 + 10 = 42 outputs which can be used for elements and indicators particular to each game.

On the Master Unit there is a circuit which will produce a pulse (Reset Power On) when the system is switched on or as a result of a sharp variation of more than 0.6 v. between the +5 v. and -12 v. lines. The circuit, functioning and connection can be seen in the next drawing.



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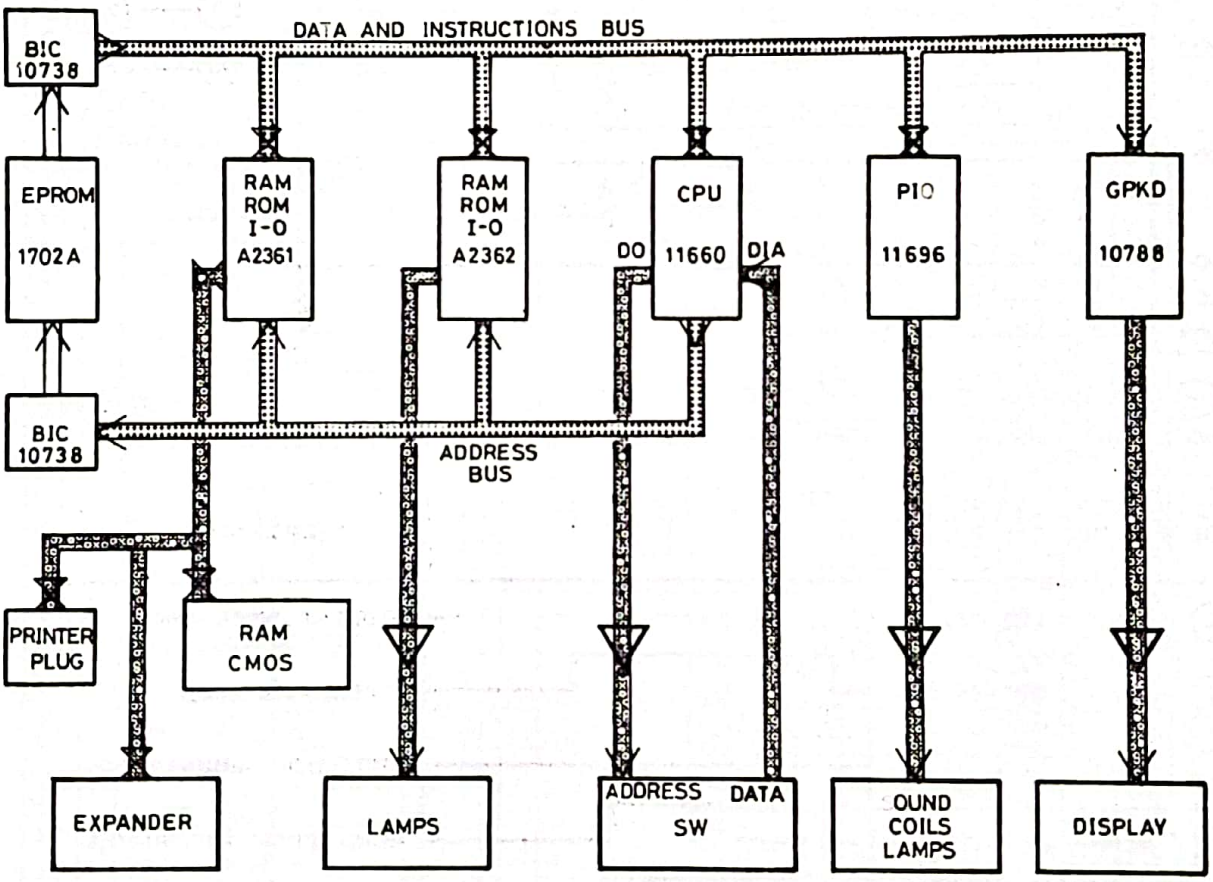
In the diagram shown below, you can see that the CPU ccntrols and addresses all the memories and peripherals, via the address and Instruction-Data buses.

All the contacts are addressed directly by the CPU via their outputs DO, and read by means of their inputs DIA. The contacts are arranged in matrix form of 16 x 4 (maximum of 64 contacts).

As the logic levels of the buses are +5 and -12 volts, and the game memory (EPROM 1702A) is TTL compatible, it is necessary to use 2 BICS (Bus Interface Circuits) in order to make both forms of working compatible to each other.



You will see that all the outputs from the Master Unit are protected by an interface (buffer 4050), in order to protect the outputs from the MOS LSI circuits. In the case of the contacts address, the mentioned interface is a chip 7404 (TTL).

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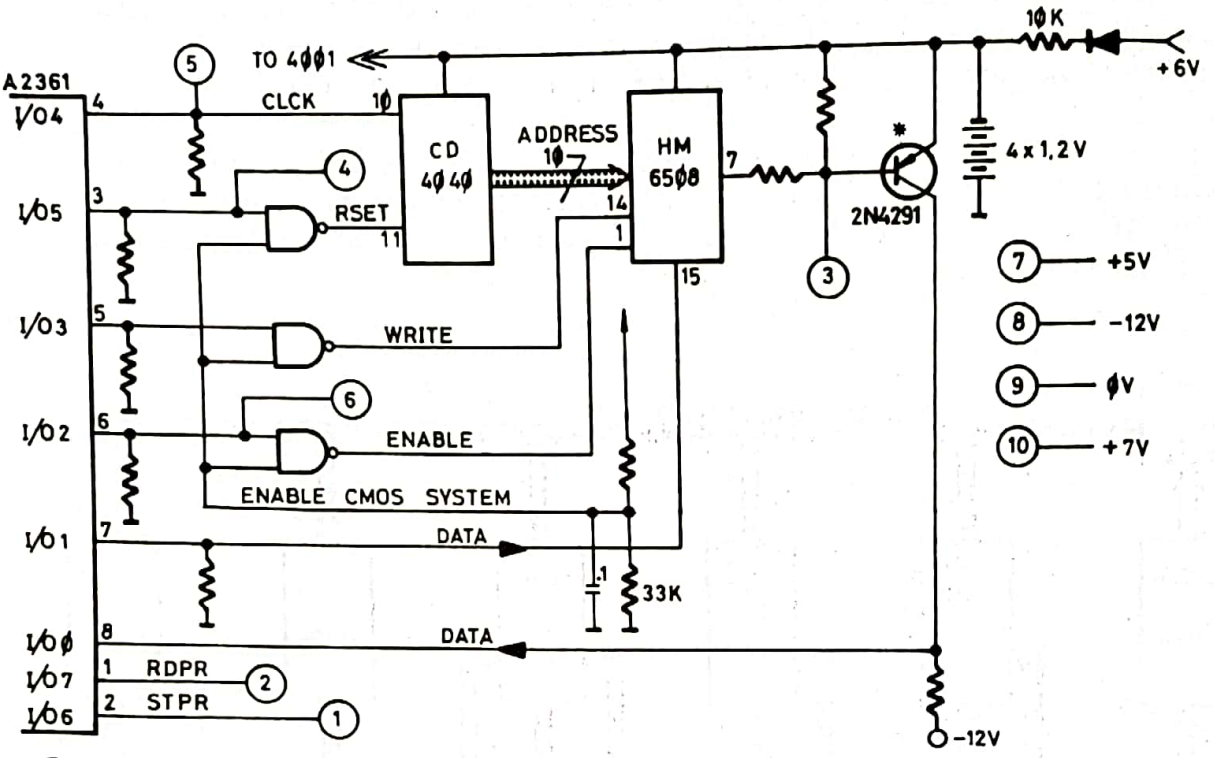
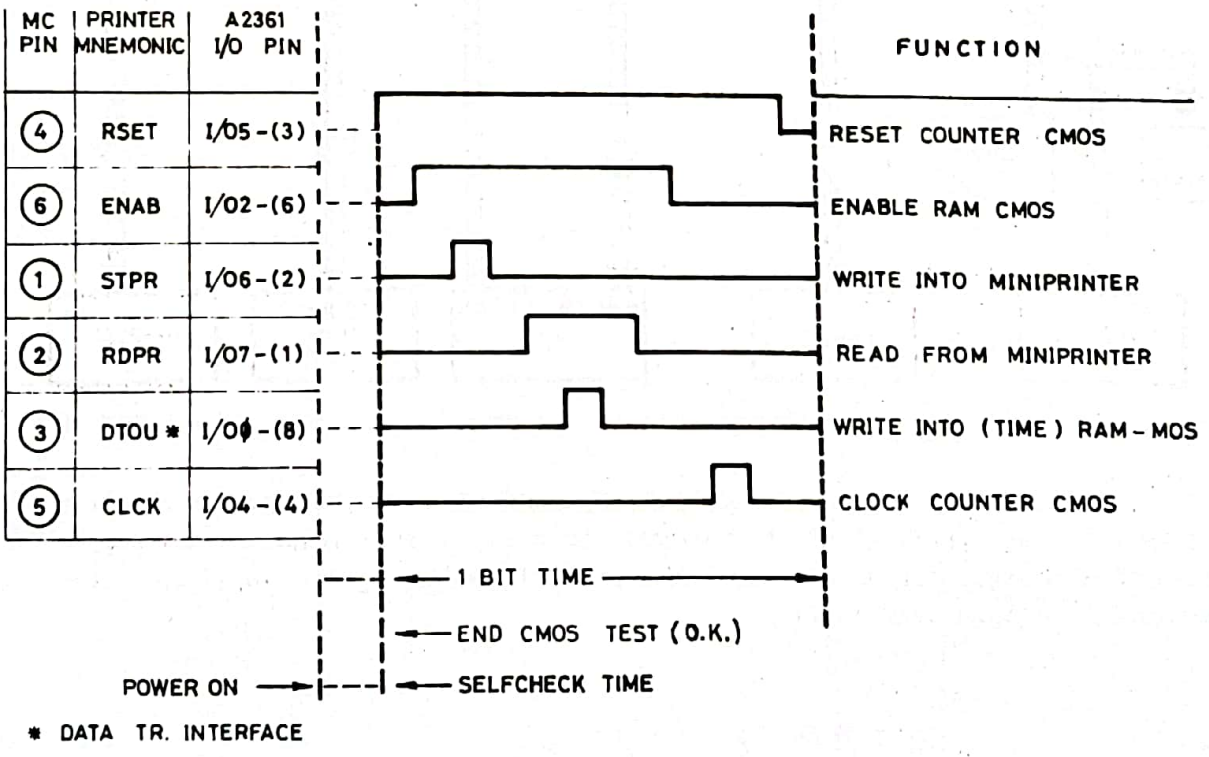
The schematic and diagram which we show below, allow you to see the form and times of working and control of the RAM CMOS memory and printer. This routine is carried out at the end of the RAM CMOS test.



(N) = PIN NUMBER IN MINIPRINTER-SOCKET (M C)

NOTE:- ALL UNSIGNED RESISTORS ARE OF 15KΩ



* DATA TR. INTERFACE

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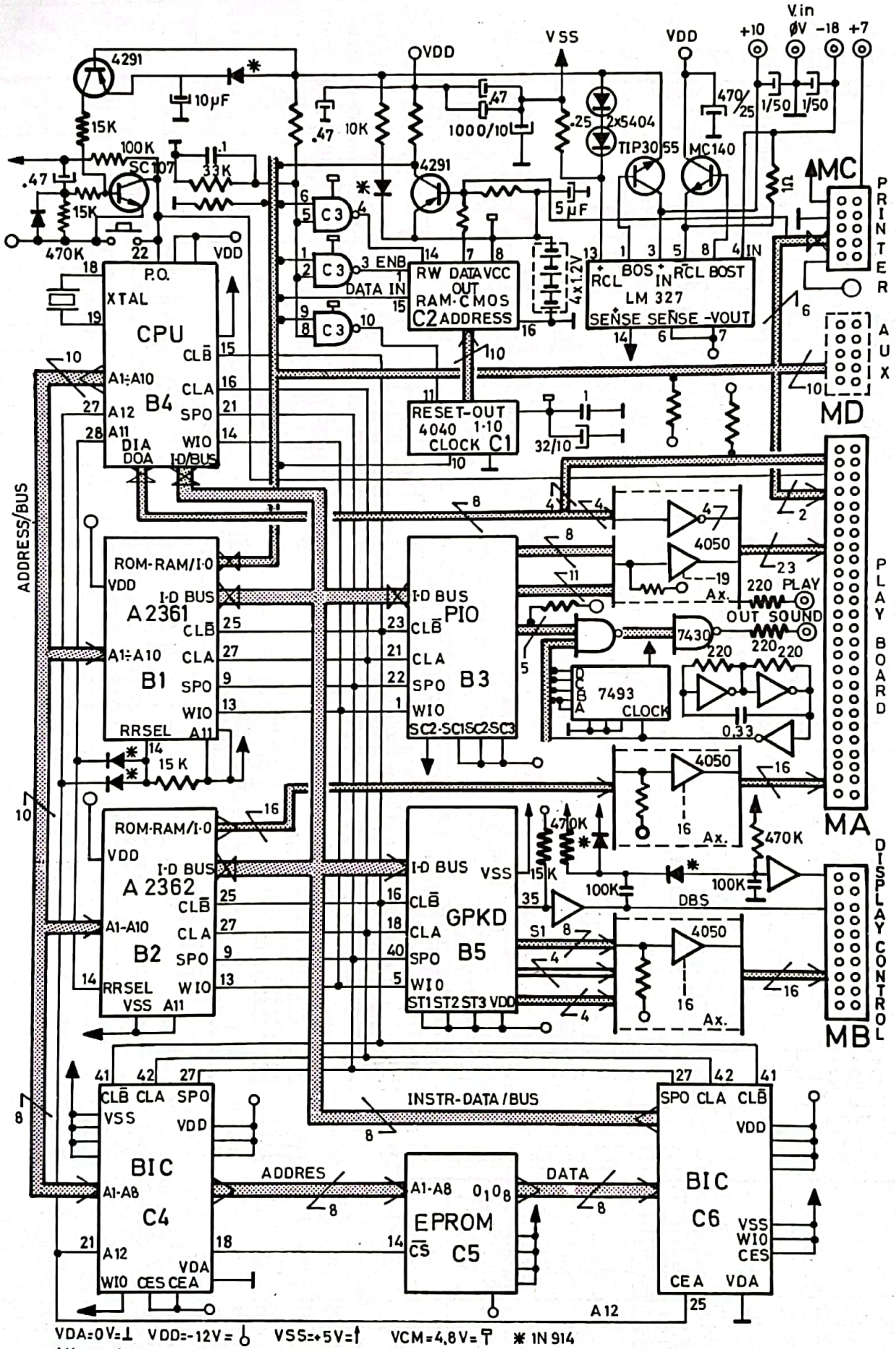
MASTER UNIT DIAGRAM



VDA=0V=⊥ VDD=-12V=⏚ VSS=+5V=↑ VCM=4,8V=⊤ * 1N 914

All unsigned resistors are equal to 15KΩ

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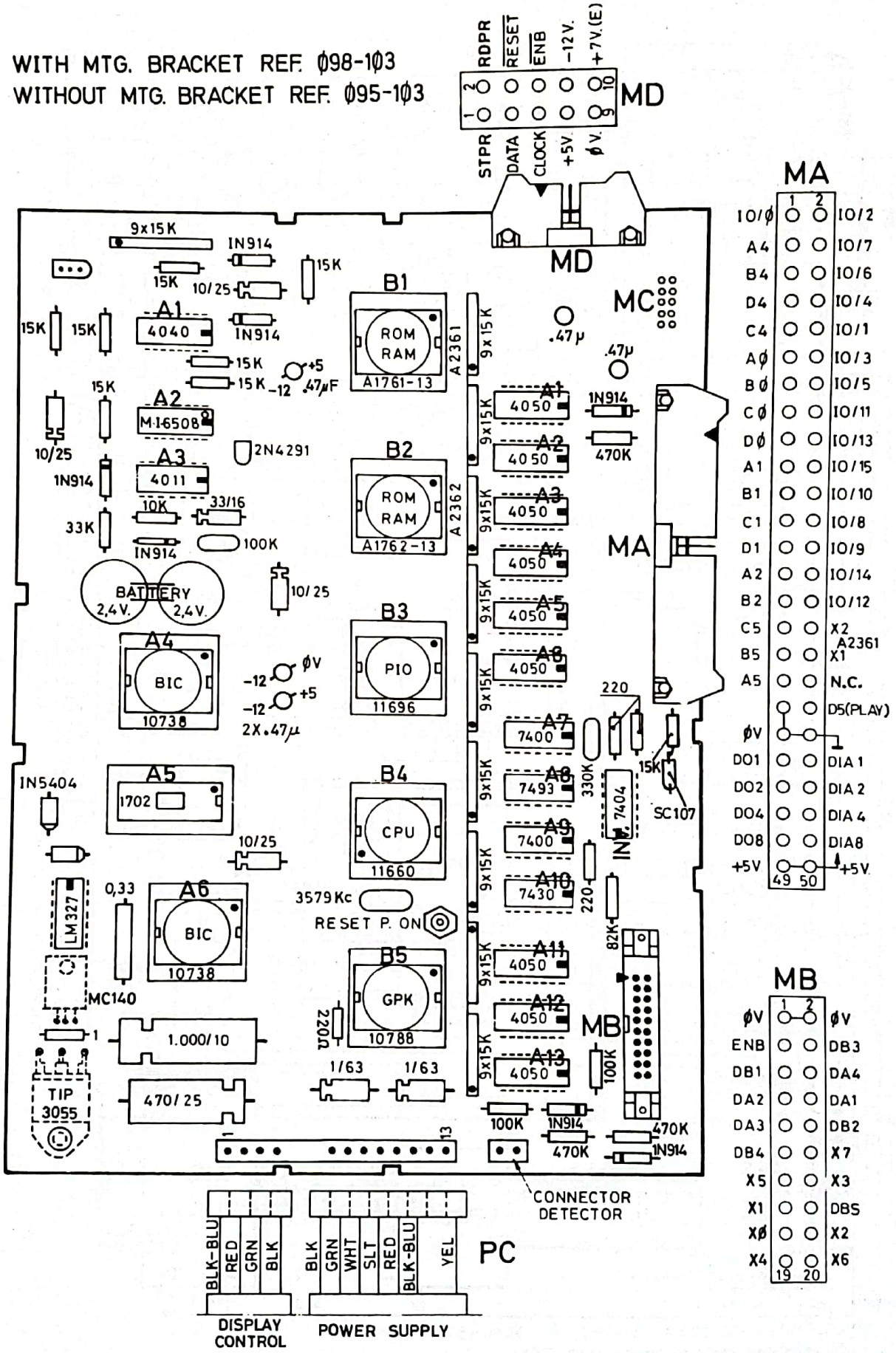
MASTER UNIT

WITH MTG. BRACKET REF. ϕ98-1ϕ3
WITHOUT MTG. BRACKET REF. ϕ95-1ϕ3



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MASTER UNIT INTERCONNECTION

CONNECT.	BUFFER			MOS			
PIN MA	PIN OUT	POSITION	PIN IN	PIN OUT	TYPE	REG. Nº	FUNCTION
1	4	A1	5	8	A 1762-13	51	LITE 51
2	1	A1	3	6	A 1762-13	54	LITE 54
3	9	A5	8	39	11696	61	BIT A BONUS
4	15	A1	14	1	A 1762-13	48	LITE 48
5	6	A6	7	4Ø	11696	62	BIT B BONUS
6	12	A1	11	2	A 1762-13	44	LITE 44
7	12	A5	11	41	11696	64	BIT C BONUS
8	1Ø	A1	9	4	A 1762-13	41	LITE 41
9	15	A5	14	42	11696	68	BIT D BONUS
1Ø	2	A2	3	7	A 1762-13	52	LITE 52
11	12	A4	11	19	11696	#F	COIL #F
12	4	A2	5	5	A 1762-13	58	LITE 58
13	15	A3	14	2Ø	11696	#E	COIL #E
14	1Ø	A2	1Ø	3	A 1762-13	42	LITE 42
15	15	A6	14	24	11696	#D	COIL #D
16	15	A2	14	39	A 1762-13	38	LITE 38
17	15	A4	14	25	11696	#C	COIL #C
18	12	A2	11	37	A 1762-13	22	N.C.
19	12	A6	11	26	11696	#B	COIL #B
2Ø	1Ø	A2	9	35	A 1762-13	28	N.C.
21	6	A5	7	27	11696	#A	COIL #A
22	2	A3	3	4Ø	A 1762-13	34	LITE 34
23	1Ø	A6	9	28	11696	#9	COIL #9
24	4	A3	5	42	A 1762-13	31	LITE 31
25	4	A	5	29	11696	#8	COIL #8
26	6	A3	7	41	A 1762-13	32	LITE 32
27	2	A6	3	3Ø	11696	#7	COIL BALL HOME
28	12	A3	11	36	A1762-13	24	NC.
29	2	A5	3	31	11696	#6	COIL KNOCKER
3Ø	1Ø	A3	9	38	A1762-13	21	LITE 21
31	4	A4	5	16	11696	74	LITE DOUBLE BONUS
32	—	—	—	42	A1761-13	X2	REJECTOR CONTROL
33	6	A4	7	18	11696	71	LITE SPECIAL
34	—	—	—	41	A1761-13	X1	EXPANDER MX-DR
35	1Ø	A4	9	17	11696	72	LITE EXTRA BALL
36	—	—	—	—	——	—	N.C.
37	—	—	—	—	——	—	ØV (VDA)
38	2	A4	3	15	11696	78	PLAY SIGNAL
39-4Ø	—	—	—	—	——	—	ØV (VDA)
41	2	INV 74Ø4	1	23	1166Ø	—	DO 1 BIT A
42				5	1166Ø	—	DIA 1 BIT A
43	8	INV 74Ø4	9	24	1166Ø	—	DO 2 BIT B
44				4	1166Ø	—	DIA 2 BIT B
45	4	INV 74Ø4	3	25	1166Ø	—	DO 3 BIT C
46				3	1166Ø	—	DIA 3 BIT C
47	1Ø	INV 74Ø4	11	26	1166Ø	—	DO 4 BIT D
48	—	—	—	2	1166Ø	—	DIA 4 BIT D
49-5Ø	—	—	—	—	——	—	5V (VSS)

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MASTER UNIT INTERCONNECTION

CONNECT.	BUFFER			MOS			
PIN MB	PIN OUT	POSITION	PIN IN	PIN OUT	TYPE 1Ø788 (GPKD)	REG Nº	FUNCTION
1	—	—	—	—	——	—	ØV (VDA)
2	—	—	—	—	——	—	ØV (VDA)
3	15	A 13	14	—	——		ENABLE (DISPLAY CONT.)
4	6	A 11	7	14	1Ø788 CA	DB 3	BIT C-DATA GROUP-B
5	4	A 11	5	12	"	DB 1	BIT A-DATA " B
6	2	A 11	3	1Ø	"	DA 4	BIT D-DATA " A
7	1Ø	A 11	9	8	"	DA 2	BIT B-DATA " A
8	12	A 11	11	7	"	DA 1	BIT A-DATA " A
9	15	A 11	14	9	"	DA 3	BIT C-DATA " A
1Ø	6	A 12	7	13	"	DB 2	BIT B-DATA " B
11	4	A 12	5	15	"	DB 4	BIT D-DATA " B
12	2	A 12	3	27	"	X7	STROBE TIME X7
13	1Ø	A 12	9	29	"	X5	STROBE TIME X5
14	12	A 12	11	31	"	X3	STROBE TIME X3
15	15	A 12	14	33	"	X1	STROBE TIME X1
16	6	A 13	7	35	"	DBS	SELECT. GROUP
17	4	A 13	5	34	"	XØ	STROBE TIME XØ
18	2	A 13	3	32	"	X2	STROBE TIME X2
19	1Ø	A 13	9	3Ø	"	X4	STROBE TIME X4
2Ø	12	A 13	11	28	"	X6	STROBE TIME X6
				1	"		SC6 TO -12V
				2	"	1/D6	TO INST. BUS
				3	"		SC7 TO -12V
				4	"	1/D7	TO INST. BUS
				5	"	W/I-O	TO INST. BUS
				6	"	1/D8	TO INST. BUS
				11	"		5V VSS
				16	"	CLKB	CLOCK B
				17	"		-12 (VDD)
				18	"	CLKA	CLOCK A
				19	"	NC	
				2Ø	"	NC	
				21	"	NC	
				22	"	NC	
				23	"	NC	
				24	"	NC	
				25	"	NC	
				26	"	NC	
				36	"	ID 3	INST. BUS
				37	"	ID 2	INST. BUS
				38	"	ID 4	INST. BUS
				39	"	ID 1	INST. BUS
				4Ø	"	SPO	INST. BUS
				41	"		SC5 TO -12V
				42	"	1/D5	INST. BUS

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MASTER UNIT INTERCONNECTION

CONNECT.	BUFFER			MOS			
PIN MC	PIN OUT	POSITION	PIN IN	PIN OUT	TYPE	REG. Nº	FUNCTION
1		——		35	A-1761-13	I/O-15	I-O EXPANDER
2		——		37	A-1761-13	I/O-13	I-O EXPANDER
3		——		39	A-1761-13	I/O-11	I-O EXPANDER
4		——		41	A-1761-13	X-1	EXPANDER MX-DR
5		——		42	A-1761-13	X-2	REJECTOR CONTROL
6		——		40	A-1761-13	I/O-10	I-O EXPANDER
7		——		38	A-1761-13	I/O-12	I-O EXPANDER
8		——		36	A-1761-13	I/O-14	I-O EXPANDER
9		——			——		ØV (VDA)
10		——			——		ØV (VDA)
MD							
1		——		2	A-1761-13	I/O-6	STPR
2		——		1	A-1761-13	I/O-7	RDPR
3		——		7	BASE SC-107	I/O-1	DATA PRINTER
4		——		3	A-1761-13	I/O-5	RESET
5		——		4	A-1761-13	I/O-4	CLOCK
6		——		6	A-1761-13	I/O-2	ENABLE
7		——			——		+5V (VSS)
8		——			——		-12V(VDD)
9		——			——		ØV(VDA)
10		——			——		+7VCC
ME							
1		——			——		ØVDC
2		——			——		+5VDC
3		——			——		+7VDC
4		——			——		ØVDC
5		——			——		N.C.
6		——			——		ØVDC
7		——			——		+7VDC
8		——			——		OUT-SOUND
9		——			——		CONTROL PLAY
10		——			——		+10VDC
11		——			——		Ø VDC
12		——			——		Ø VDC
13		——			——		-18 VDC
		——			——		
MF		——			——		
1		——			——		ØVDC LOGIC DETECTOR
2		——			——		+5VDC LOGIC DETECTOR

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ADDRESS BUS INTERCONEXION

ADDRESS BUS	CPU	A 1761	A 1762	PIO	GPKD	EPROM FROM BIC	ADDRESS BIC FROM BUS	ADDRESS BIC TO EPROM
A/B 1	38	28	28	—	—	3	34	10
A/B 2	37	29	29	—	—	2	33	11
A/B 3	36	3Ø	3Ø	—	—	1	32	12
A/B 4	35	31	31	—	—	21	31	13
A/B 5	34	32	32	—	—	2Ø	38	6
A/B 6	33	33	33	—	—	19	37	7
A/B 7	32	34	34	—	—	18	36	8
A/B 8	31	2Ø	2Ø	—	—	17	35	9
A/B 9	3Ø	23	23	—	—	—	—	—
A/B 1Ø	29	21	21	—	—	—	—	—
A/B 11	28	⊣14	14	—	—	—	—	—
A/B 12	27	⊣14	—	—	—	14	21	18
						I/ DATA BIC		
A/B 12 IS ENABLE OF EPROM AND I/DATA BIC.						EPROM	FROM BUS	TO EPROM
							25	

INSTRUCTION-DATA BUS INTERCONEXION

I-D BUS	CPU	A 1761	A 1762	PIO	GPKD	EPROM	I/DATA BIC FROM BUS	I/DATA BIC TO EPROM
CLKA	16	27	27	21	18	—	42	—
CLKB̄	15	25	25	13	16	—	41	—
W I/O	14	13	13	1	—	—	29	—
I/D 1	1Ø	16	16	1Ø	39	4	10	34
I/D 2	12	17	17	11	37	5	11	33
I/D 3	13	18	18	12	36	6	12	32
I/D 4	11	19	19	13	38	7	13	31
I/D 5	6	15	15	2	42	8	6	38
I/D 6	7	1Ø	1Ø	4	2	9	7	37
I/D 7	8	11	11	6	4	1Ø	8	36
I/D 8	9	12	12	8	6	11	9	35
SPO	21	9	9	22	4Ø	—	—	—

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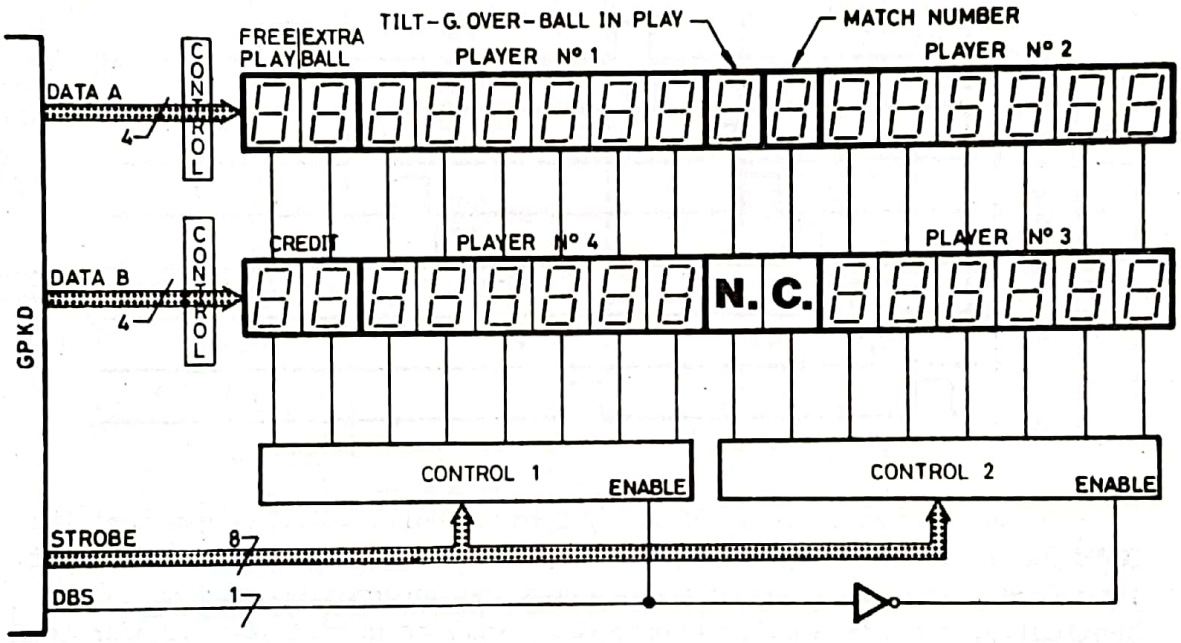
DISPLAY CONTROL UNIT

5.3 This unit is in charge of controlling all the displays and indicators housed in the lite box of the machine.

It receives the information coming from the GPKD (to be fourd in the Master Unit), in two groups of data.

Below you will see a diagram showing the working of this unit, with hypothetical indicators. (In order to simplify the diagram, let us assume that the 32 indicators are 7 segment displays).



The data corresponding to the first line of indicators arrives sequentially via the group "DATA A", and parallelly time-wise the data for the second line of indicators arrives via group "DATA B".

The line DBS automatically changes its state with every full cycle of the 8 Strobe lines; whilst DBS is low, control 1 will be active, and when it changes its state, control 2 is active.

In the following diagram of times, you can see the working of DBS, STROBE and DATA A and DATA B.

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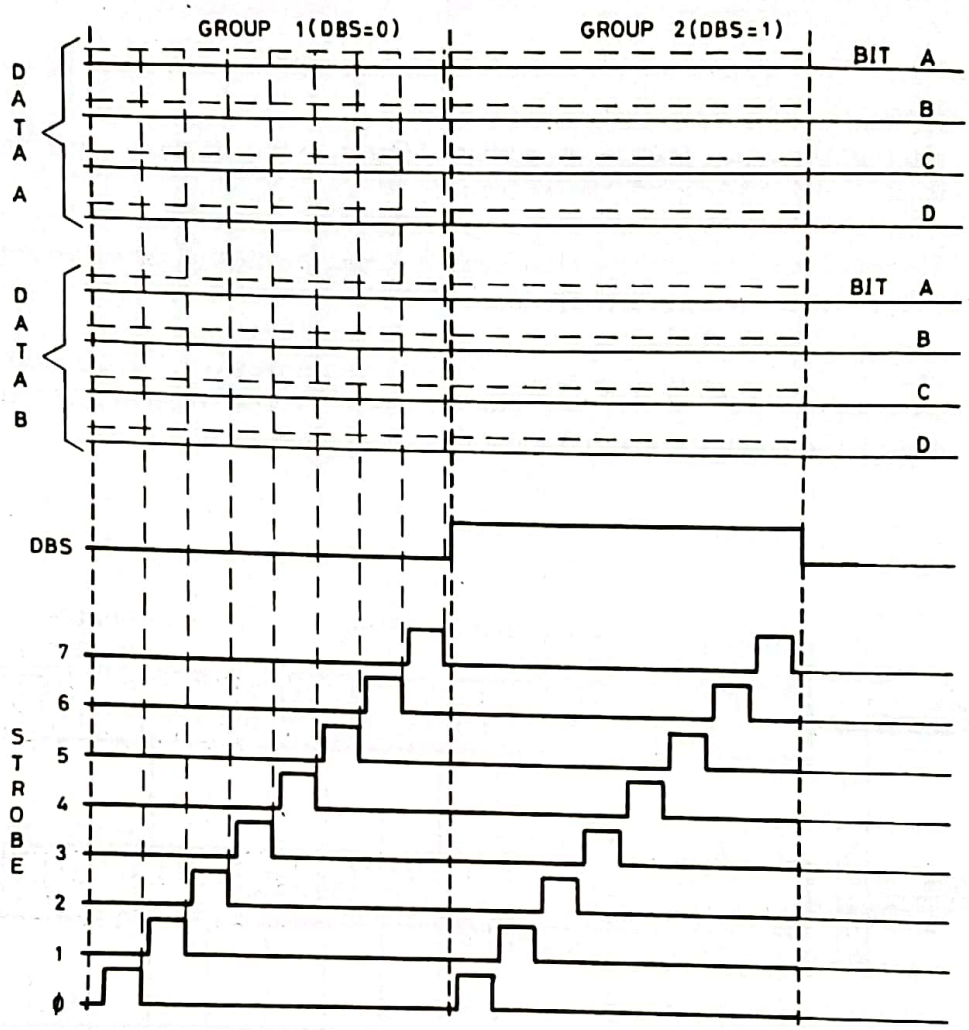

In the schematic of the Display Control Unit, you will see that the SCANNING lines used to control the displays, have a driver as the output interface. The lines during whose times the information must be shown statically, include a pulse former which will be used as a clock for the latches which have to "catch" the data in the corresponding time; for these cases, the data come straight from the unit, without being decoded.

In order to control the segments of the displays, each group (DATA A and DATA B) is decoded by means of a 7448 chip, and with a driver inserted in its output (integrated in the Transistor Array chips CA 3081).

The following diagram shows the groups of data and scanning lines corresponding to each indicator, and on the following two pages we have shown the board assembly and theoretical schematics with all the relevant indications concerning functions and forms of connection.

The indications (XAN) and (XBN) and DAN and DBN correspond to the drivers or control signals specified in the DISPLAY CONTROL DIAGRAM.

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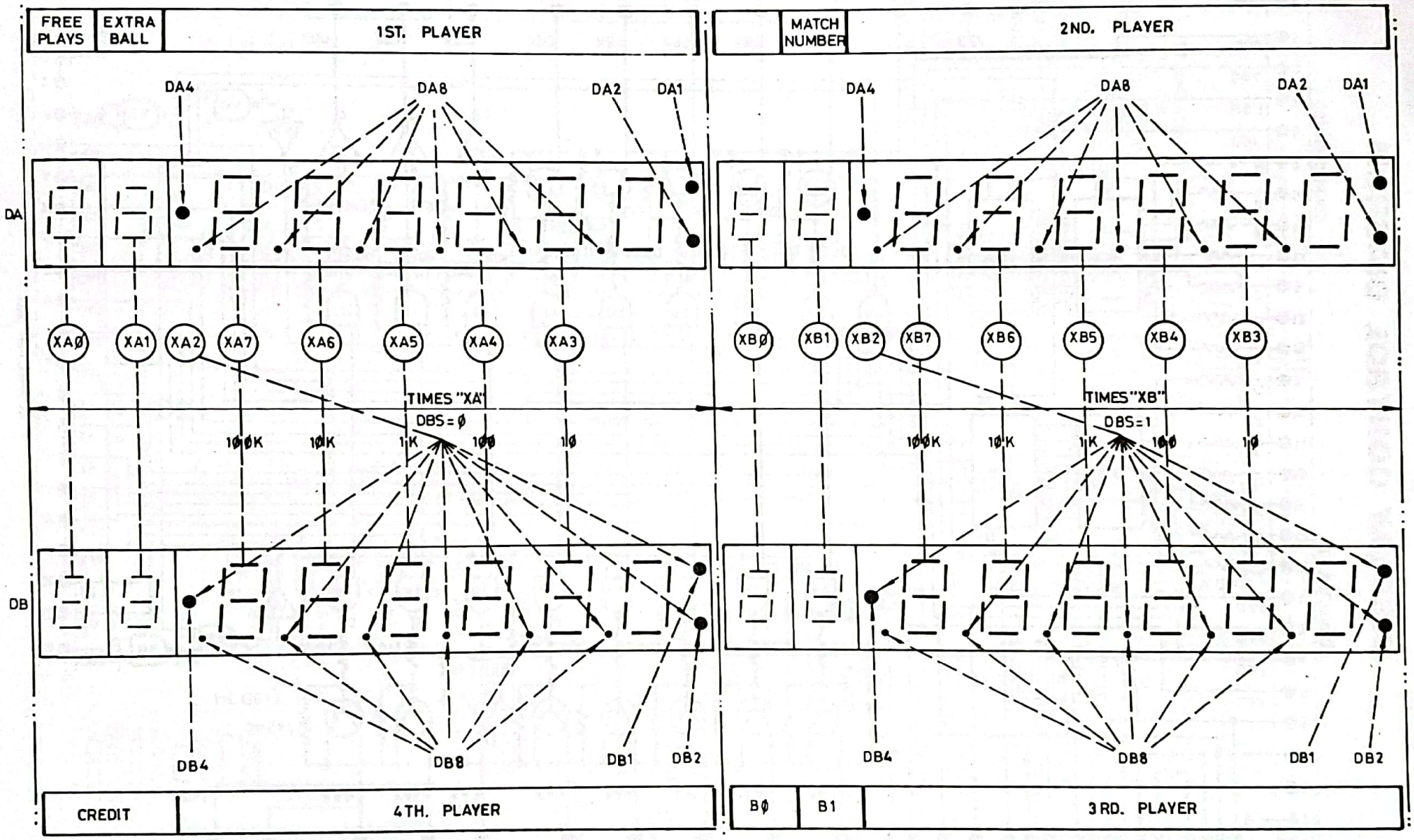
FREE PLAYS
EXTRA BALL
1ST. PLAYER
MATCH NUMBER
2ND. PLAYER
DA4
DA8
DA2
DA1
DA
XAØ
XA1
XA2
XA7
XA6
XA5
XA4
XA3
TIMES "XA"
DBS = Ø
1ØØK
1ØK
1K
1ØØ
1Ø
DB
DB4
DB8
DB1
DB2
XBØ
XB1
XB2
XB7
XB6
XB5
XB4
XB3
TIMES "XB"
DBS = 1
CREDIT
4TH. PLAYER
BØ
B1
3RD. PLAYER

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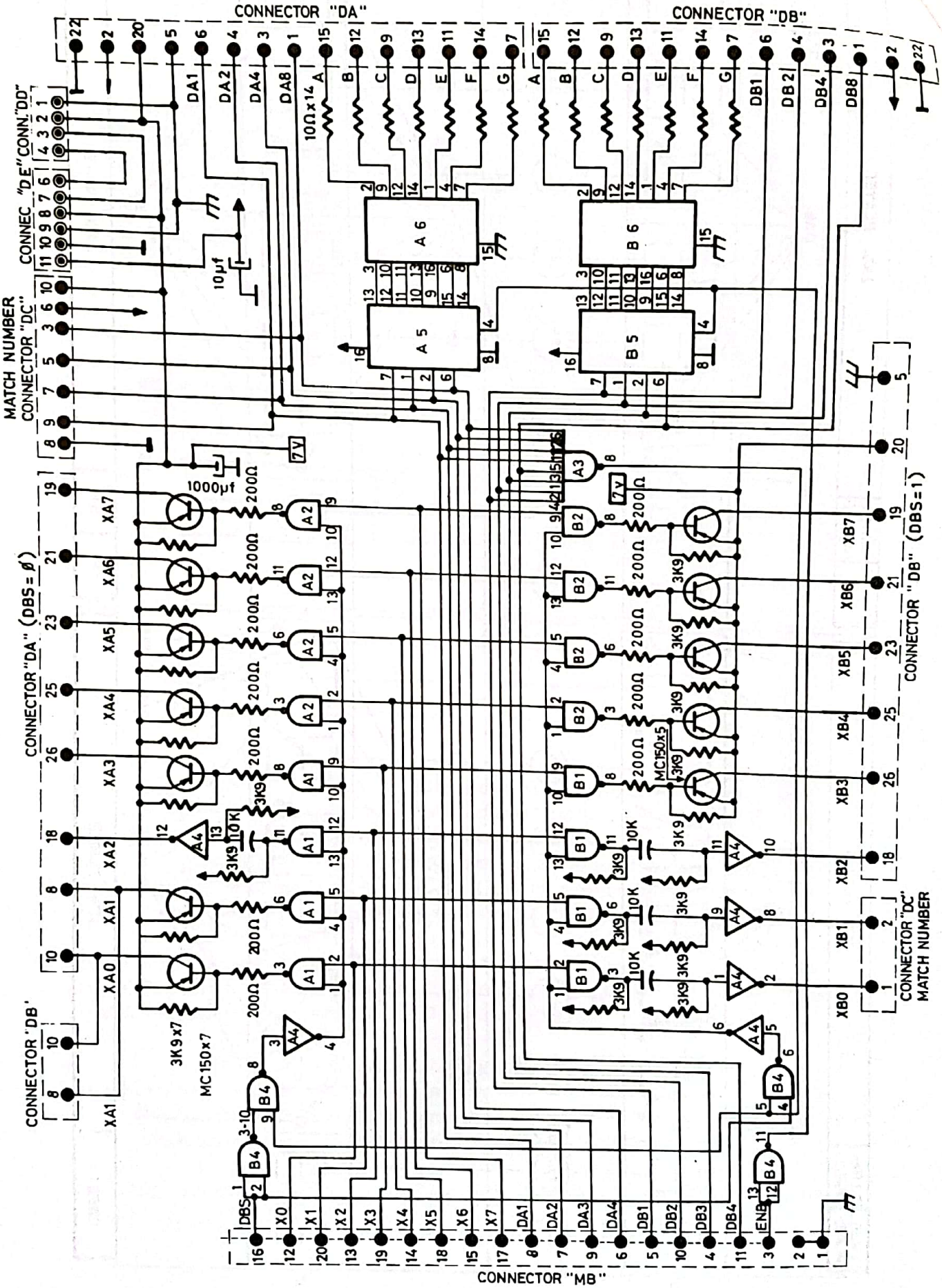
DISPLAY CONTROL DIAGRAM



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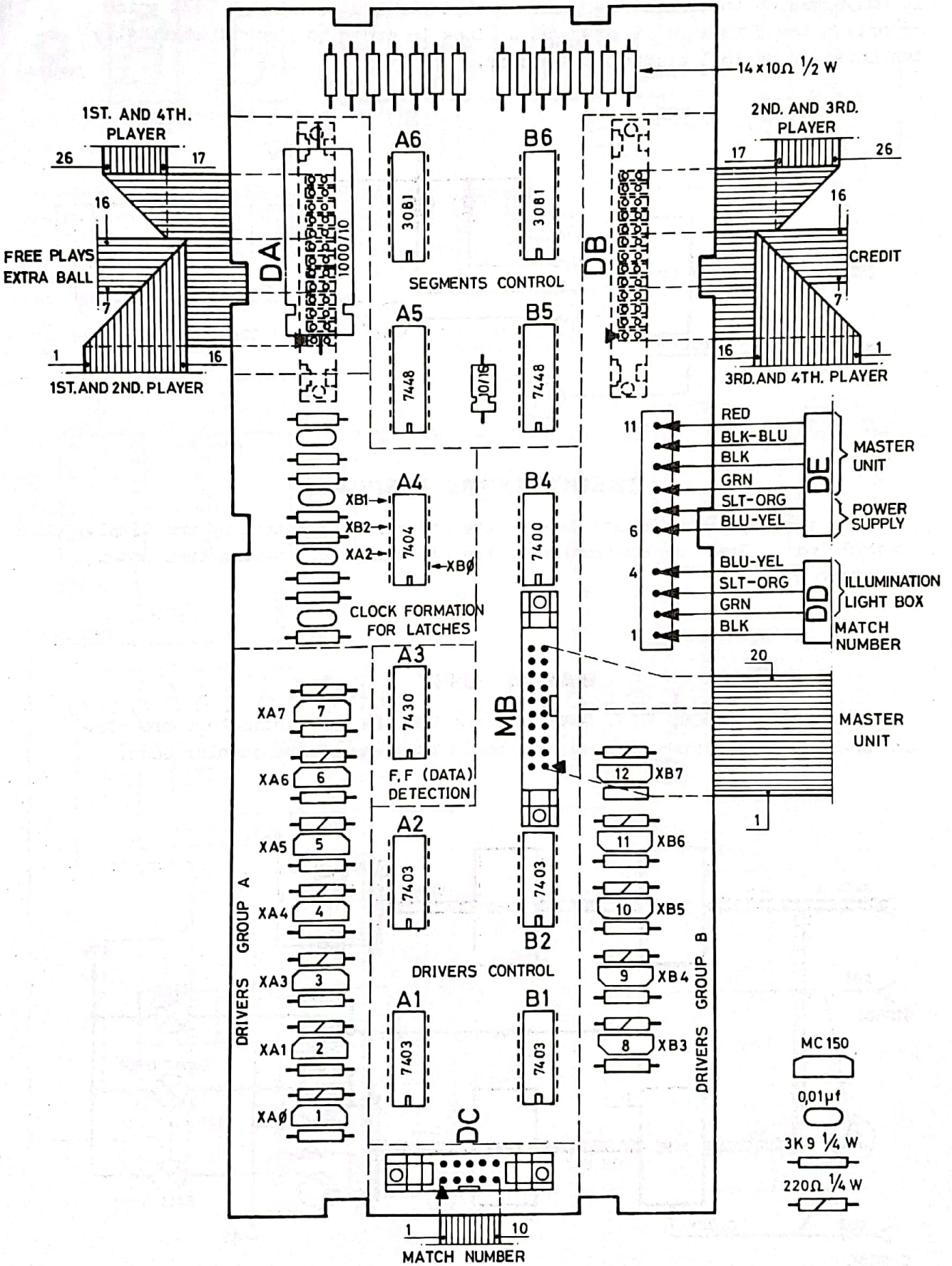
DISPLAY CONTROL Ø95-1Ø4



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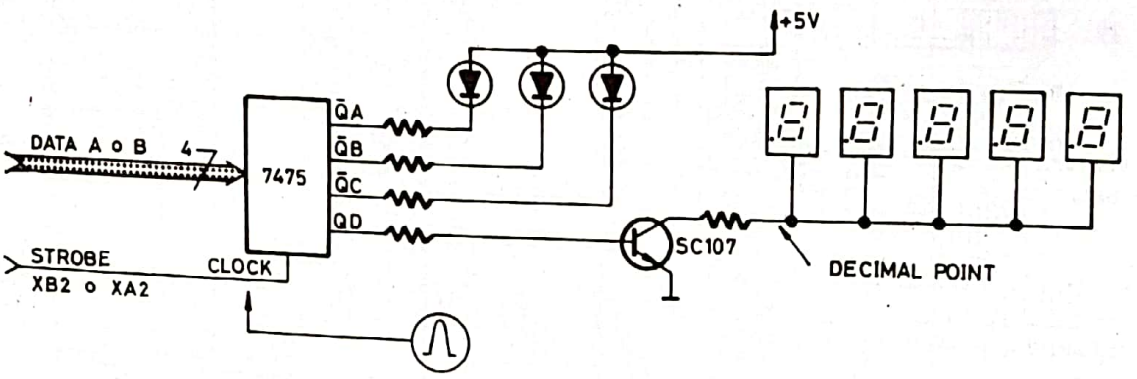
5-4 PLAYER DISPLAYS

The Display Unit 095-105 is activated by the Display Control Unit and it only remains to mention that each unit incorporates a latch 7475 which memorizes the data when it receives a clock in order to control statically the Leds and decimal points in the unit.

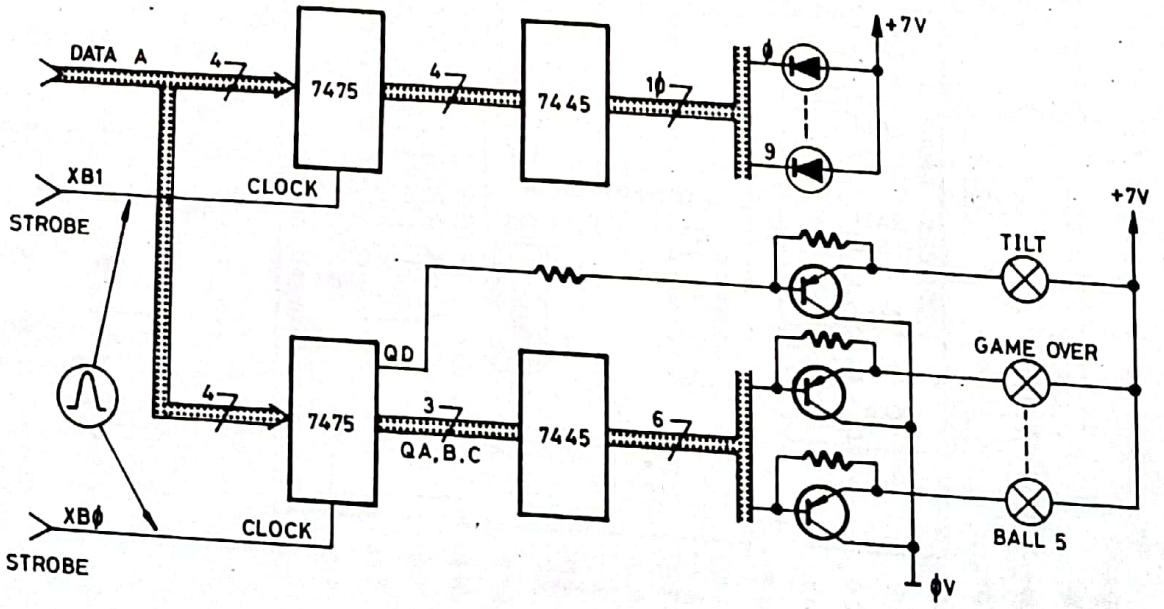


CREDIT-EXTRA DISPLAYS

The displays 095-106 and 095-207 are controlled directly by the Display Control Unit. They are controlled in the standard way, as described under paragraph 5.3.

MATCH UNIT

The MATCH NUMBER, TILT, GAME OVER and BALL IN PLAY indicators are static and the same system is used here as in the case of the counter Leds.



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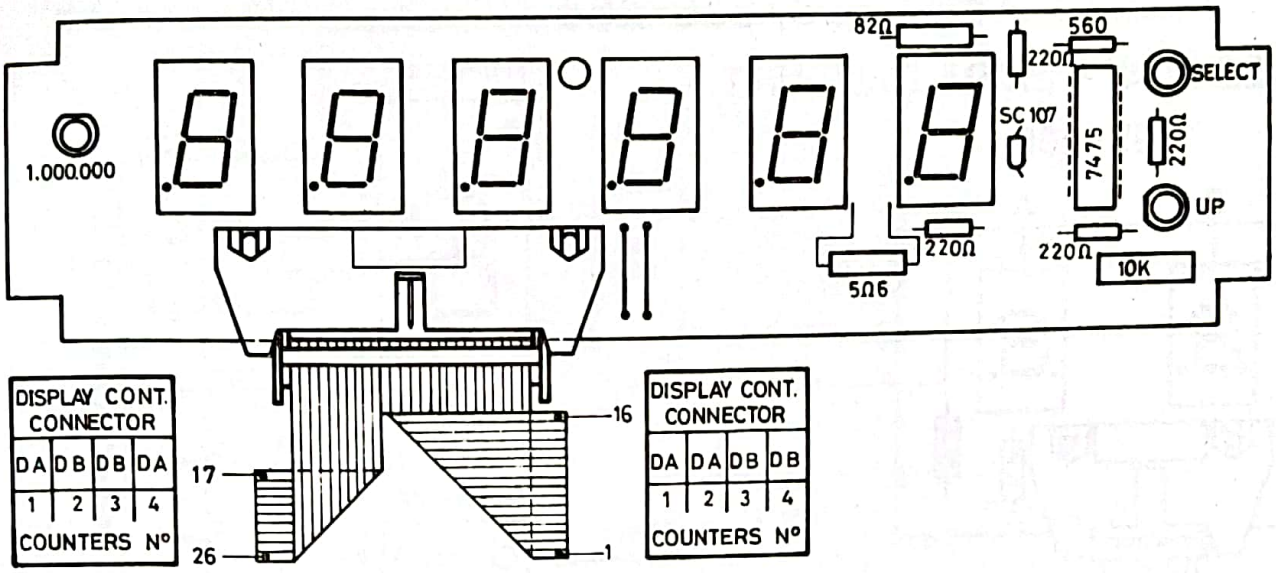
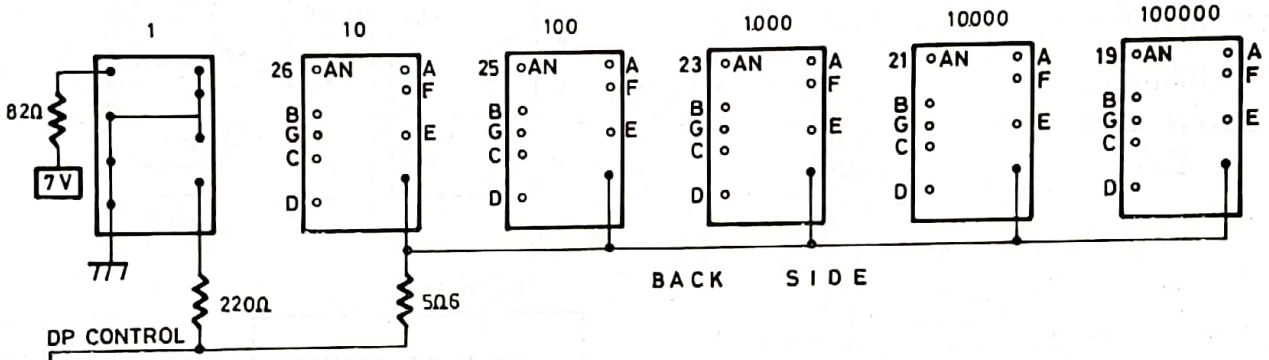
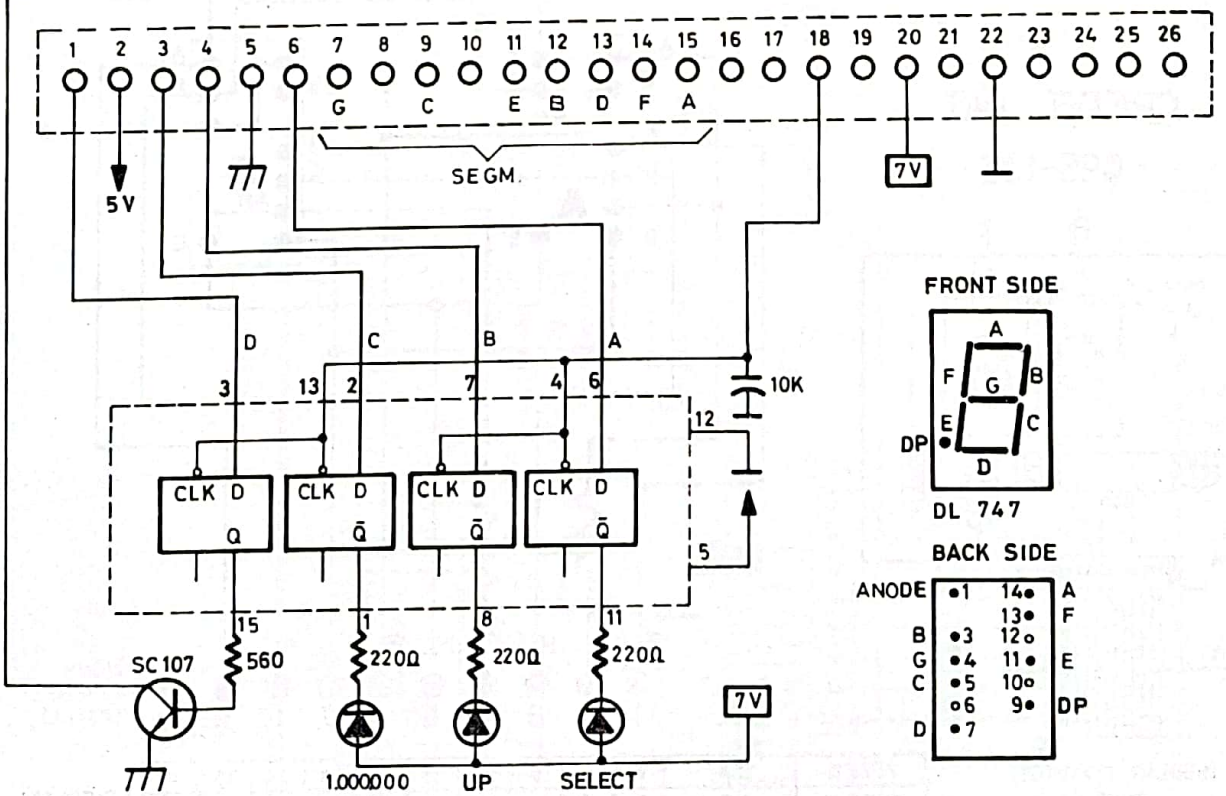
COUNTER UNIT Ø95-1Ø5







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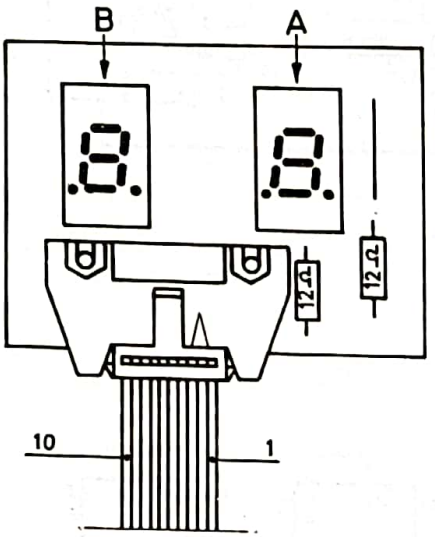
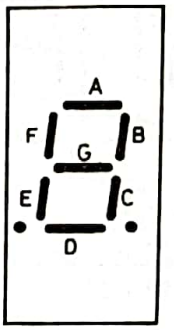
CREDIT, FREE PLAY AND EXTRA BALL UNIT
Ø95-1Ø6/Ø95-2Ø6

FREE PLAY - EXTRA BALL UNIT
Ø95-2Ø6



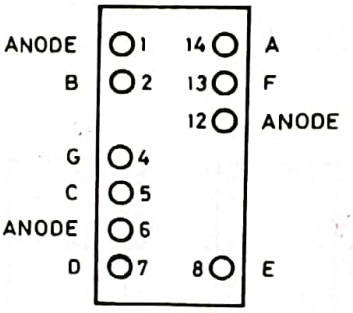
DISPLAY CONTROL
DA

FRONT SIDE

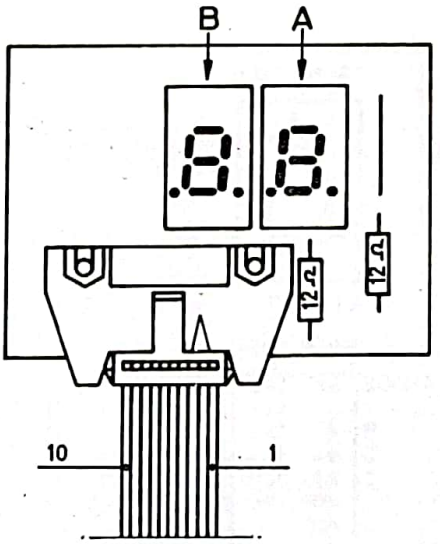


DL 7Ø7

BACK SIDE

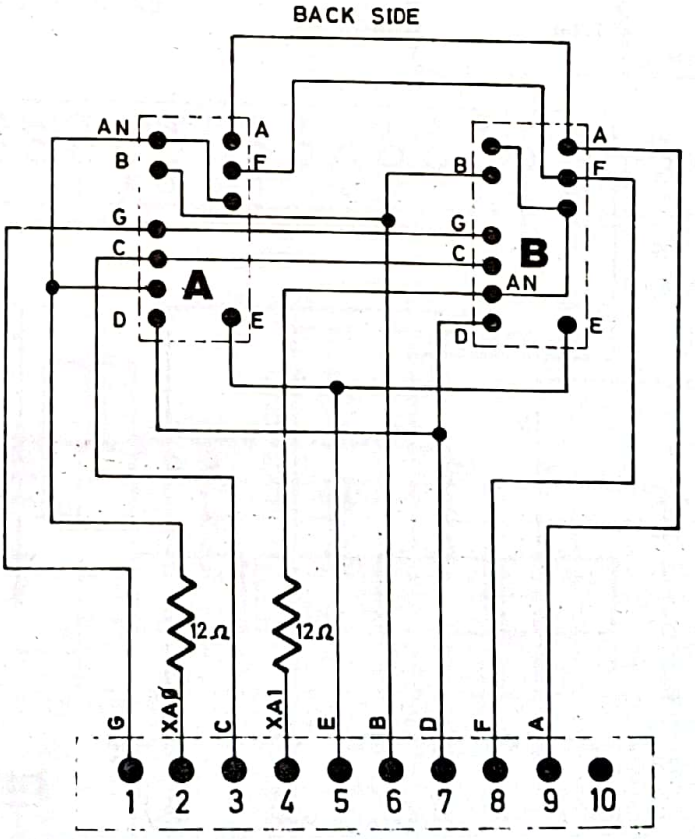


CREDIT UNIT
Ø95-1Ø6



DISPLAY CONTROL
DB

BACK SIDE



FP/EB	DA	7	8	9	10	11	12	13	14	15	16	DISPLAY CONTROL
CREDIT	DB	7	8	9	10	11	12	13	14	15	16	
UNIT	CONNECTOR	CONNECTOR POSITION										

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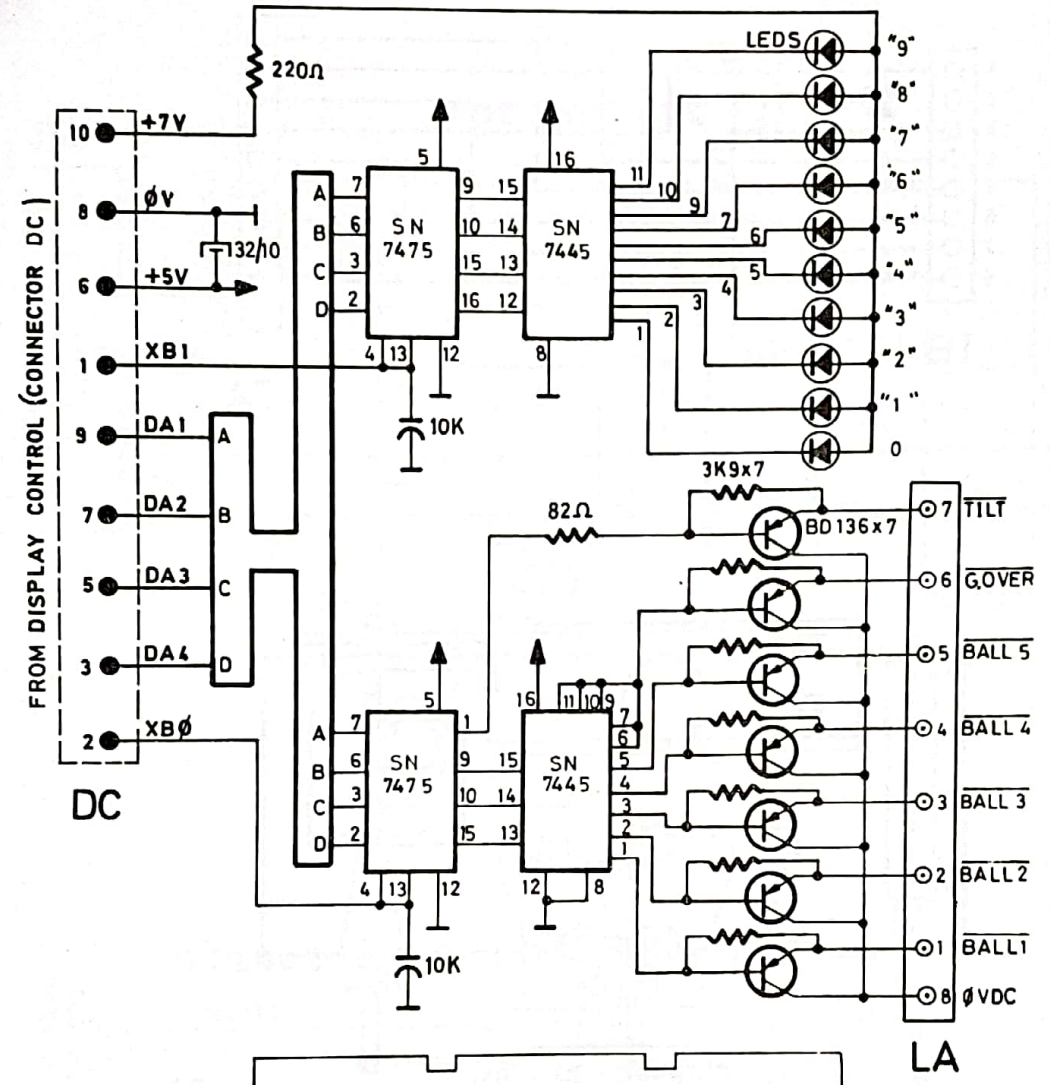
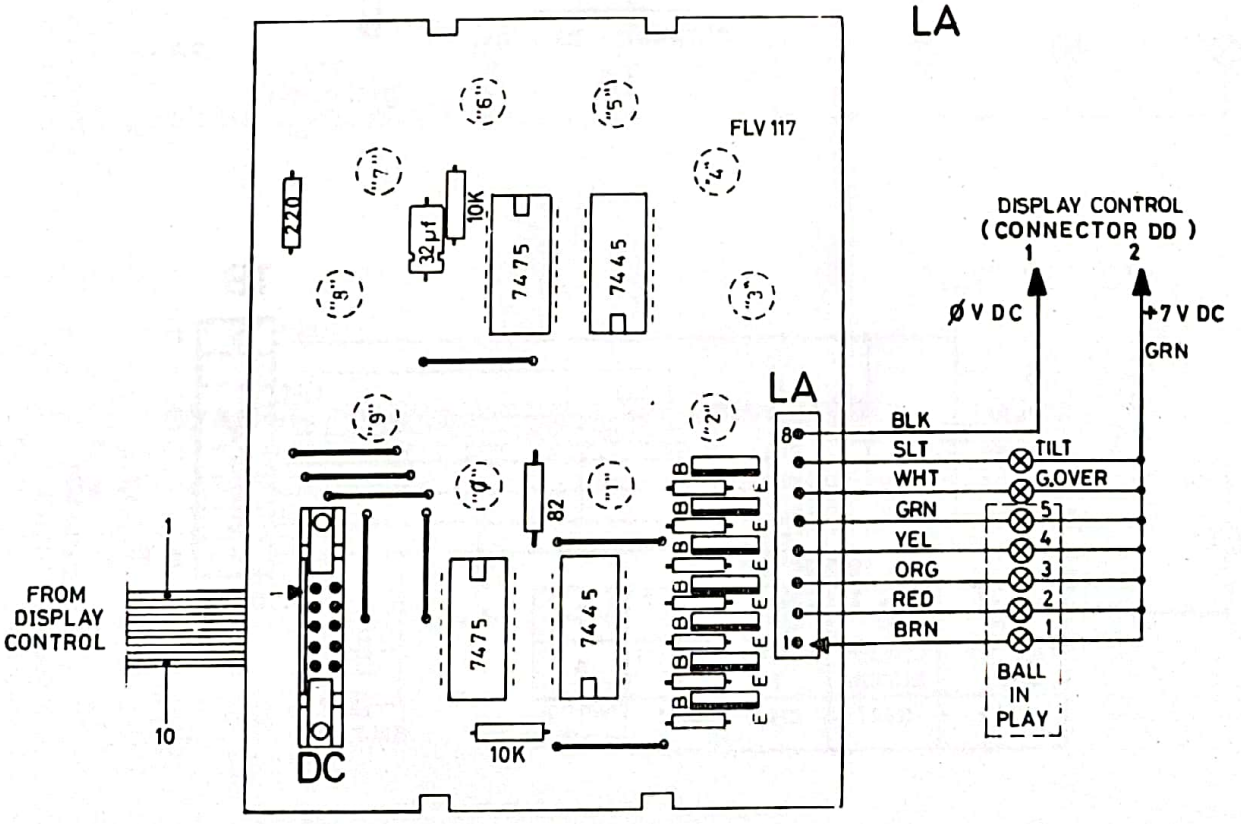
MATCH NUMBER UNIT Ø95-1Ø8 AND CHANGE ILLUMINATION





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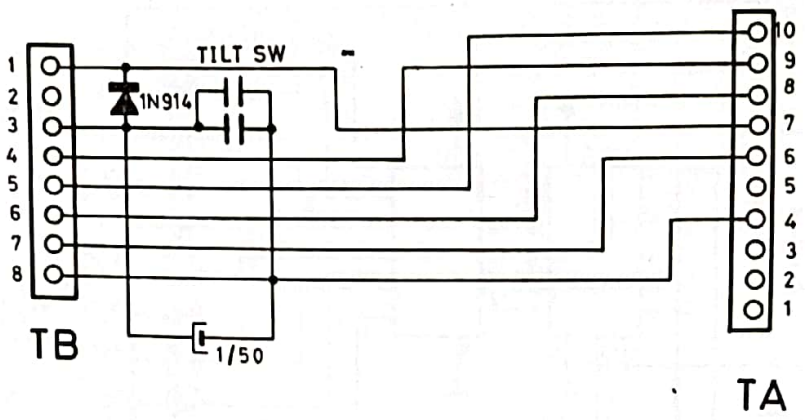
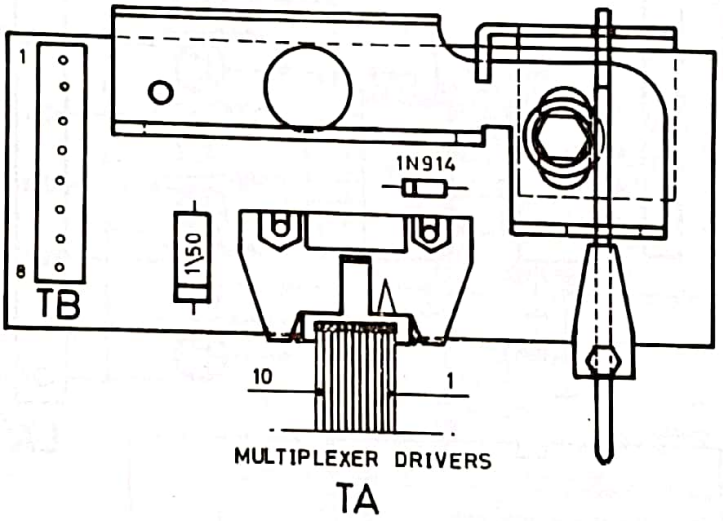
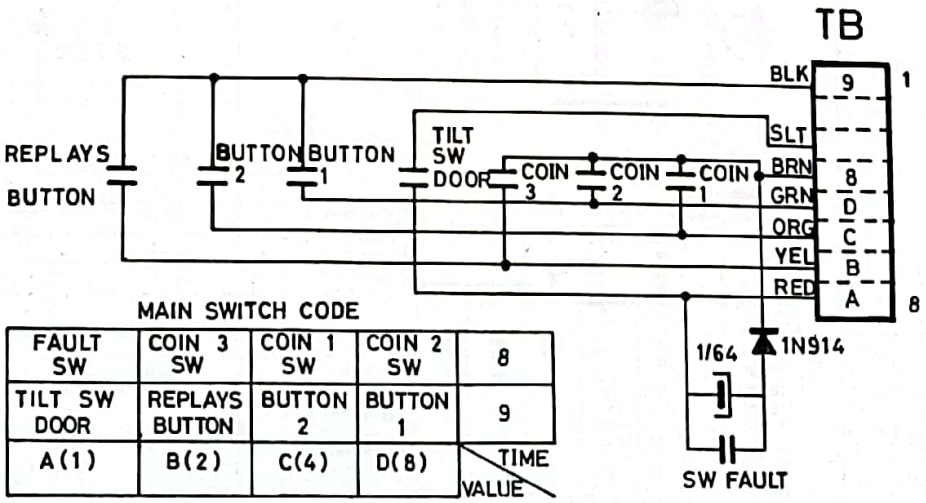
5-5 TILT UNIT Ø98-1Ø1 AND FRONT DOOR







MAIN SWITCH CODE

FAULT SW	COIN 3 SW	COIN 1 SW	COIN 2 SW	8
TILT SW DOOR	REPLAYS BUTTON	BUTTON 2	BUTTON 1	9
A(1)	B(2)	C(4)	D(8)	TIME / VALUE

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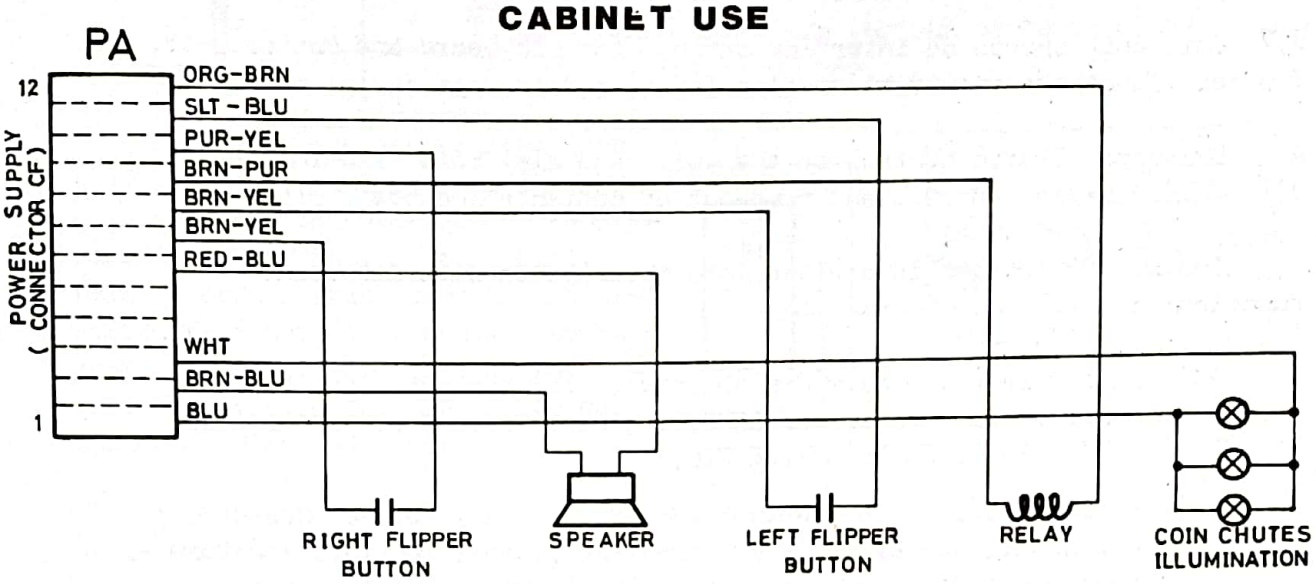
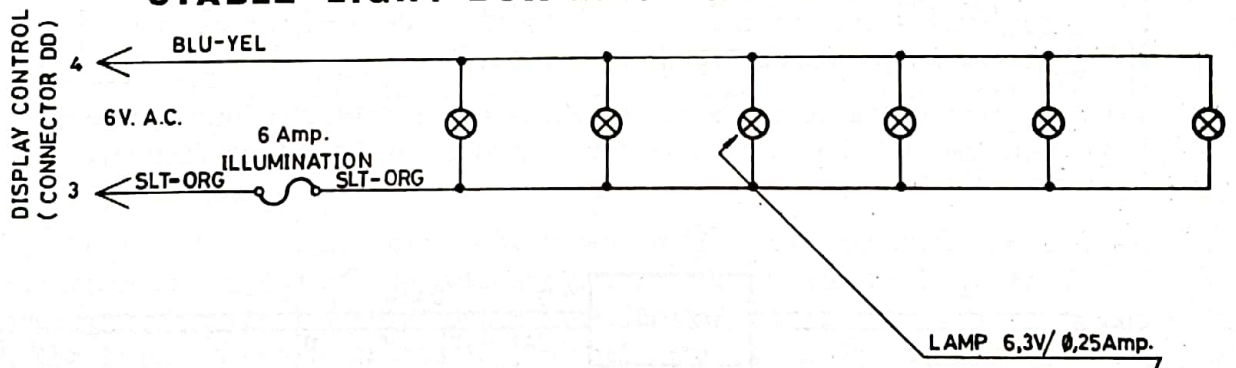
5-6 PLAYBOARD, LIGHT BOX ILLUMINATION AND CABINET USE

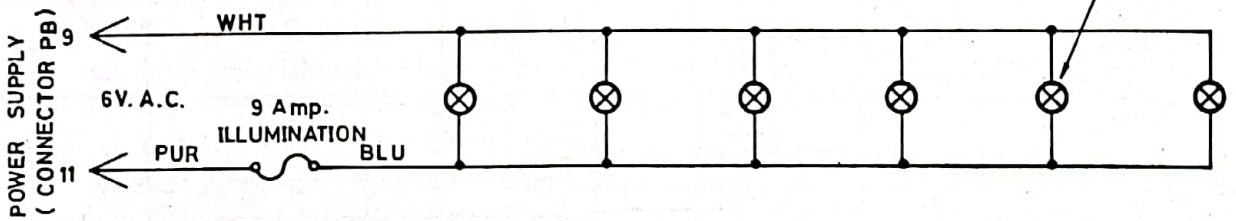
CABINET USE



STABLE LIGHT BOX ILLUMINATION



STABLE PLAYBOARD ILLUMINATION



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MULTIPLEXER DRIVERS

5.7 This unit serves as interface between the playboard and Master Unit. Two main functions should be distinguished in this unit :

A) Drivers: Static control of the coils and playfield illumination.
B) Multiplexer: Address and read-out of contacts and power play.

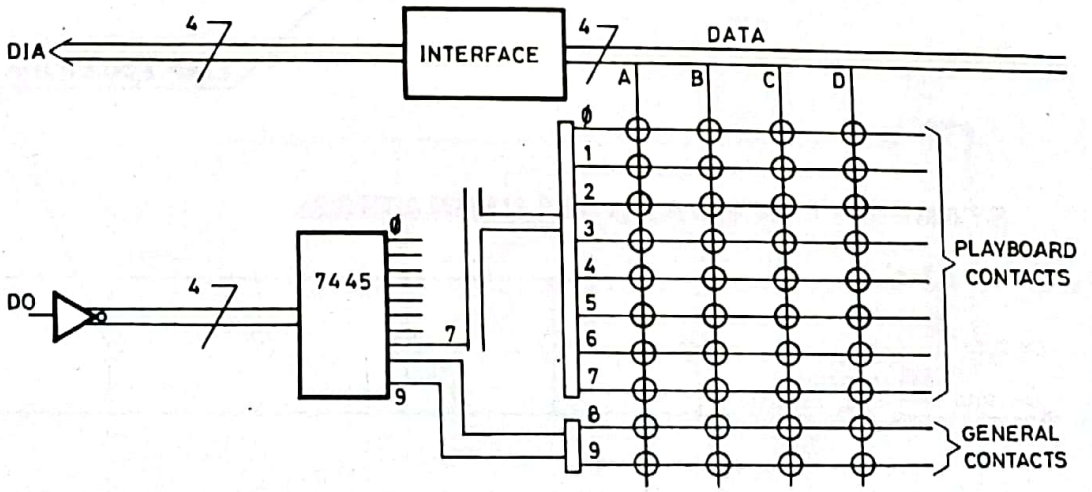
The Driver section is divided into three parts with different functions :

A1) Coil Drivers: There are 10 drivers for the coils and they use a Darlington transistor BDX33C. These drivers are controlled by 10 of the outputs from PIO.

A2) Bonus Drivers: The indicators corresponding to the Bonuses are controlled by BD138 drivers (PNP 1 amp), regulated in turn by the outputs from the decoders 7445, which receive their signal from group 7 of the outputs from PIO.

A3) Lamp Drivers: 14 of the outputs from A2362 have, in this unit, as many drivers MC140 (NPN 1 amp) to control the lamps. Group 8 of the outputs from the PIO are used to control the "constant indicators" (Bits A, B and C) and to control the game relay (driver and relay situated in the power supply board). The constant indicators - Extra Ball (EB), Special (SP) and Double Bonus (DB) - are controlled by other MC140 drivers, as can be seen from the circuitry of this unit.

B) All the contacts are read in groups of 4; selecting each group with one of the 10 outputs from the decoder 7445 (see figure).



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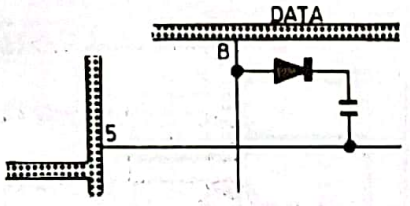
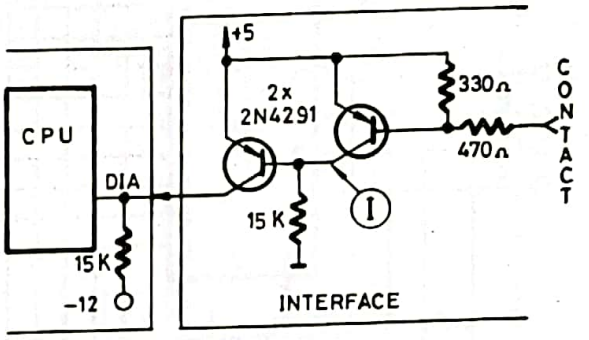
Each circle over the intersection of lines, represents a contact and its form of connection is detailed in the following example :

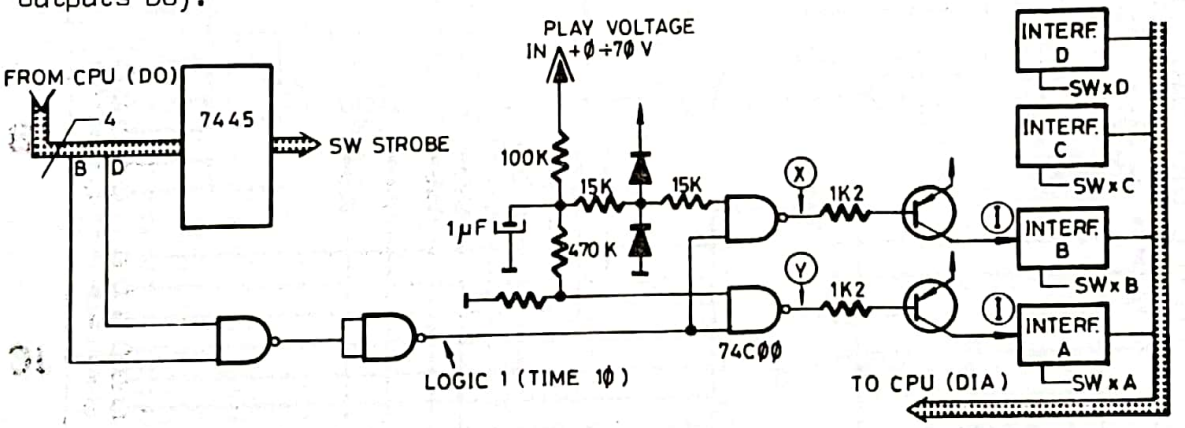


The diode mounted on each contact avoids various lines remaining interconnected when there are various contacts closed at the same time.

The interface between the Data lines from the contacts and the CPU inputs (DIA), is formed by 2 transistors 2N4291 (PNP) (for each bit). This interface transforms the information from the +5 v. contact (open) or Ø v. contact (closed), to the levels required by the DIA inputs on the CPU (+5 and -12 volts).



The reading of the state of the power play, coil drivers and coils is shown in the following circuit, as though it dealt with a couple of contacts working over Bits A and B in time 10 (code sent by the CPU via its outputs DO).



In the above figure the point shown as (I) corresponds to the base-collector connection of the relevant interface. As can be seen, this circuit is functioning only during time 10 and will give at points X and Y, the logic values indicated in the following table, in relation to the power play value. These readings will reach the processor and in each case, this latter will act and decide in consequence.

(X)	(Y)	Power Play Voltage	Functional Cause	Indication on Self-Check Table
1	1	IN < 4 volts	No voltage or Short	2.4.6 or X.4.4.
1	Ø	4 < IN <15 volts	Normal consumption	2.4.5 or . . .
Ø	1	ERROR	Faulty reading	
Ø	Ø	IN> 15 volts	No consumption (Open)	X.4.7.

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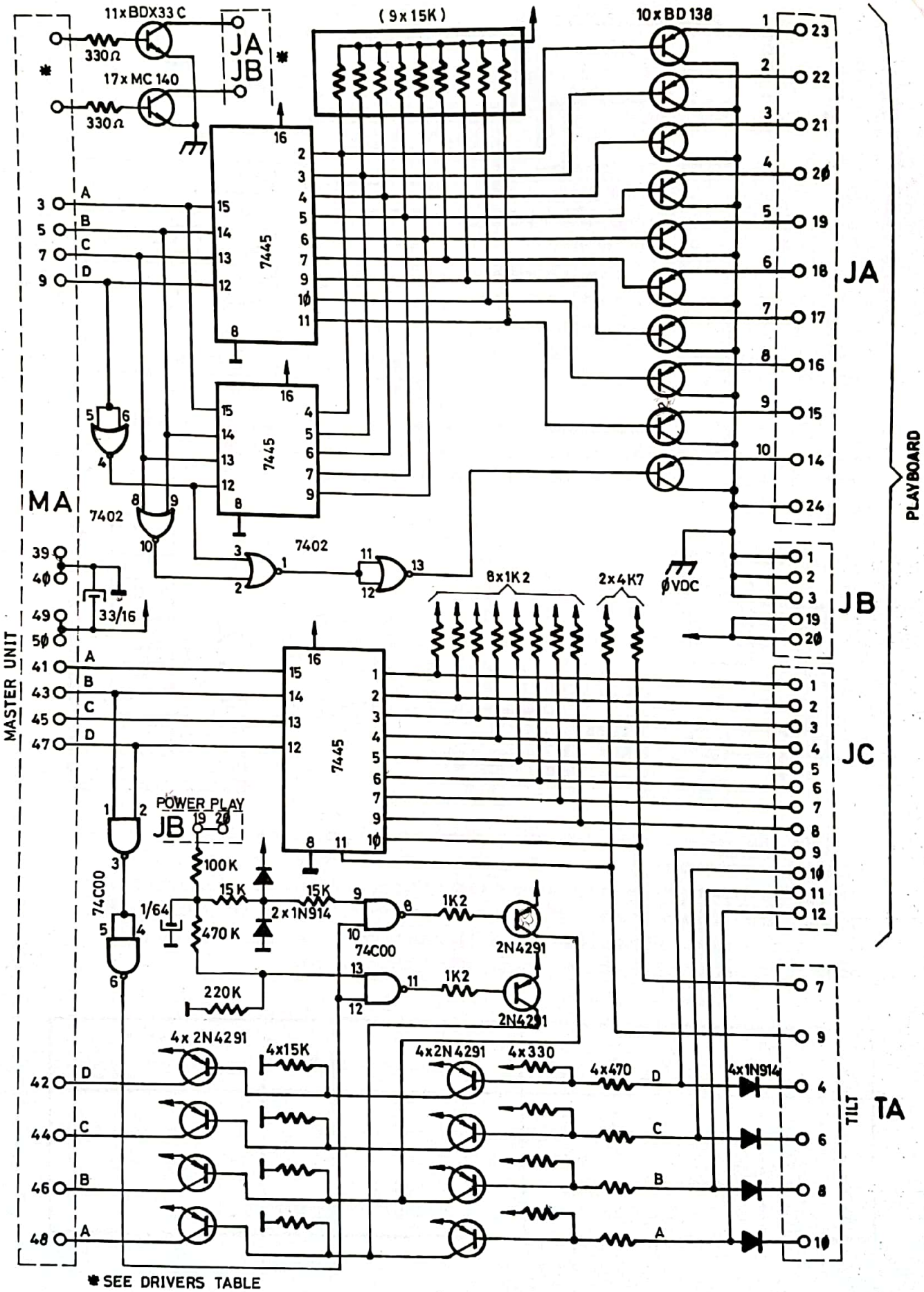
MULTIPLEXER DRIVERS ø95-113
- DIAGRAM -



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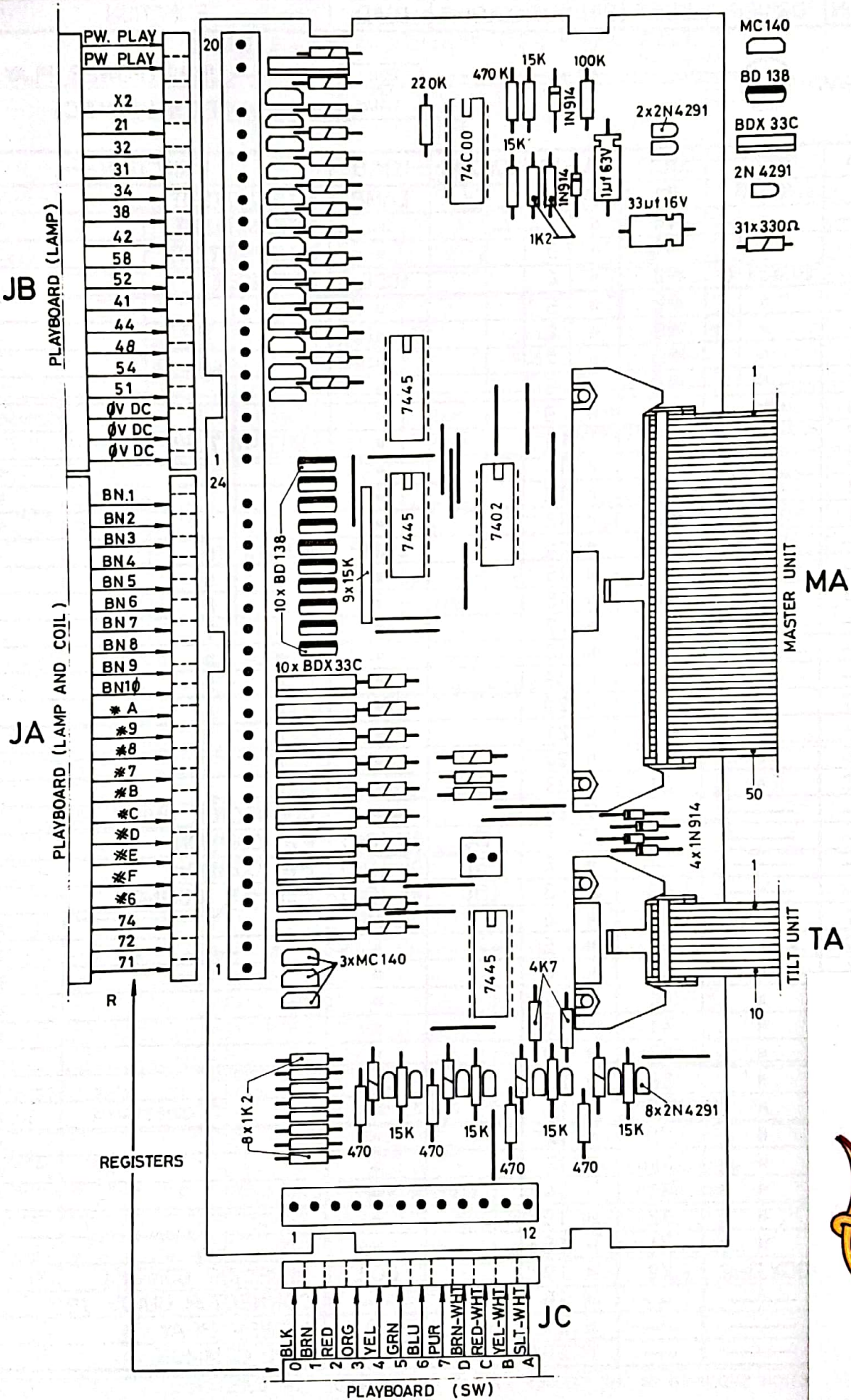
MULTIPLEXER DRIVERS ϕ95-113
- ASSEMBLY -



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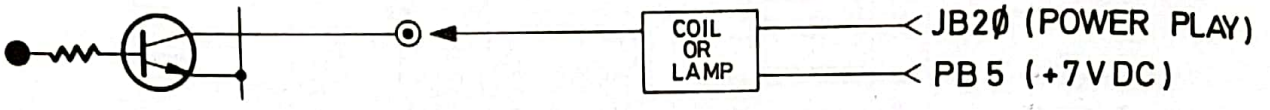
DRIVERS TABLE (UNIT Ø95-113)

MODEL ----------/----------

PIN IN	DRIVER	REGIST.	PIN OUT	COLOUR	LOAD	FUNCTION



MA	TIPE	CODE	JA–JB	COLOUR	LOAD	FUNCTION
31	MC 14Ø	72	JA 1		LAMP	INTERMITTENT *
33	"	74	" 2		"	INTERMITTENT *
35	"	71	" 3		"	INTERMITTENT *
29	BDX33-C	#6	" 4		1COIL	KNOCKER
11	"	#F	" 5		"	*
13	"	#E	" 6		"	*
15	"	#D	" 7		"	*
17	"	#C	" 8		"	*
19	"	#B	" 9		"	*
27	"	#7	" 1Ø		"	BALL RETURN
25	"	#8	" 11		"	*
23	"	#9	" 12		"	*
21	"	#A	" 13		"	*
—	BD138	—	" 14		LAMP	BONUS 1Ø
—	"	—	" 15		"	" 9
9	"	68	" 16		"	" 8
—	"	—	" 17		"	" 7
—	"	—	" 18		"	" 6
—	"	—	" 19		"	" 5
7	"	64	" 2Ø		"	" 4
—	"	—	" 21		"	" 3
5	"	62	" 22		"	" 2
3	"	61	" 23		"	" 1
—	———	—	JA 24		———	CONNECTOR GUIDE JA
—	———	—	JB 1	BL	ØV (DC)	PW COMMON
—	———	—	" 2	BL	ØV (DC)	PW COMMON
—	———	—	" 3	BL	ØV (DC)	FLIPPER COMMON
1	MC 14Ø	51	" 4		LAMP	*
2	"	54	" 5		"	*
4	"	48	" 6		"	*
6	"	44	" 7		"	*
8	"	41	" 8		"	*
1Ø	"	52	" 9		"	*
12	"	58	" 1Ø		"	*
14	"	42	" 11		"	*
16	"	38	" 12		"	*
22	"	34	" 13		"	*
24	"	31	" 14		"	*
26	"	32	" 15		"	*
3Ø	"	21	" 16		"	*
32	BDX33-C	X2	" 17		COIL	REJECTOR CONTROL
—	———	—	" 18	———	———	CONNECTOR GUIDE JB
—	———	—	" 19	YEL	+40 V	POWER PLAY
—	———	—	" 2Ø	YEL	+40 V	COIL COMMON

* FUNCTION SPECIFIED IN THE SERVICE MANUAL ON THE MODEL IN QUESTION.

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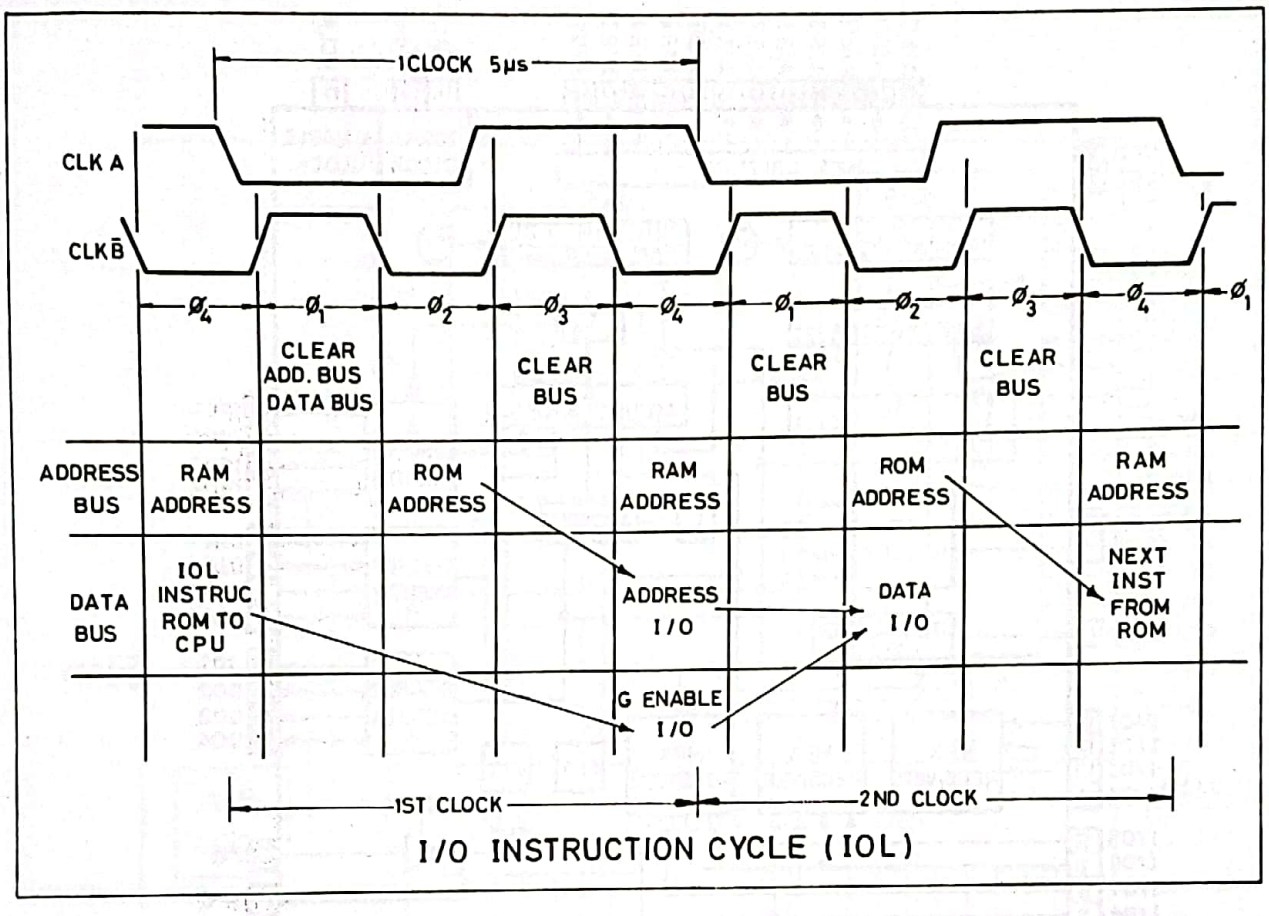
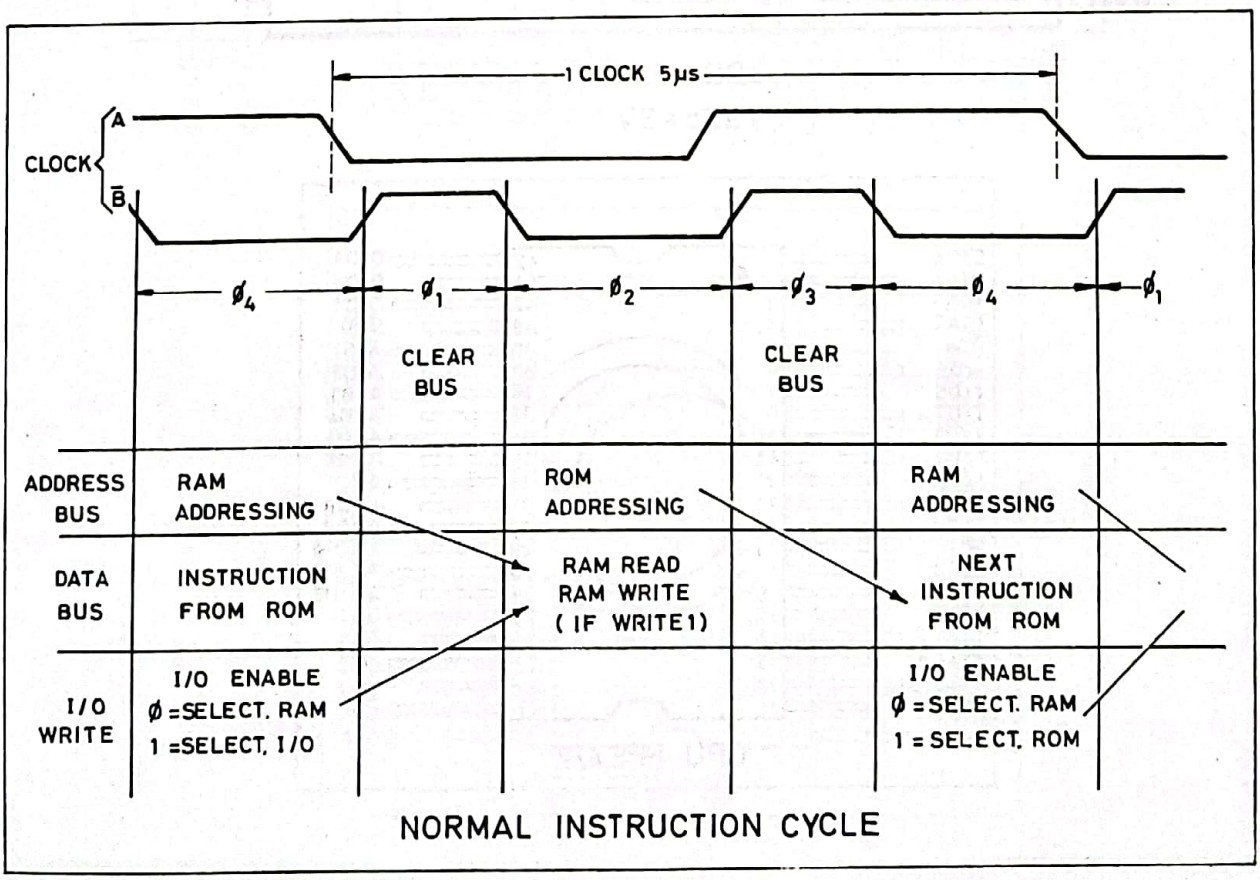
SECTION 6

TIME BASE DIAGRAM PPS-4/2 FAMILY



I/O INSTRUCTION CYCLE (IOL)



NORMAL INSTRUCTION CYCLE

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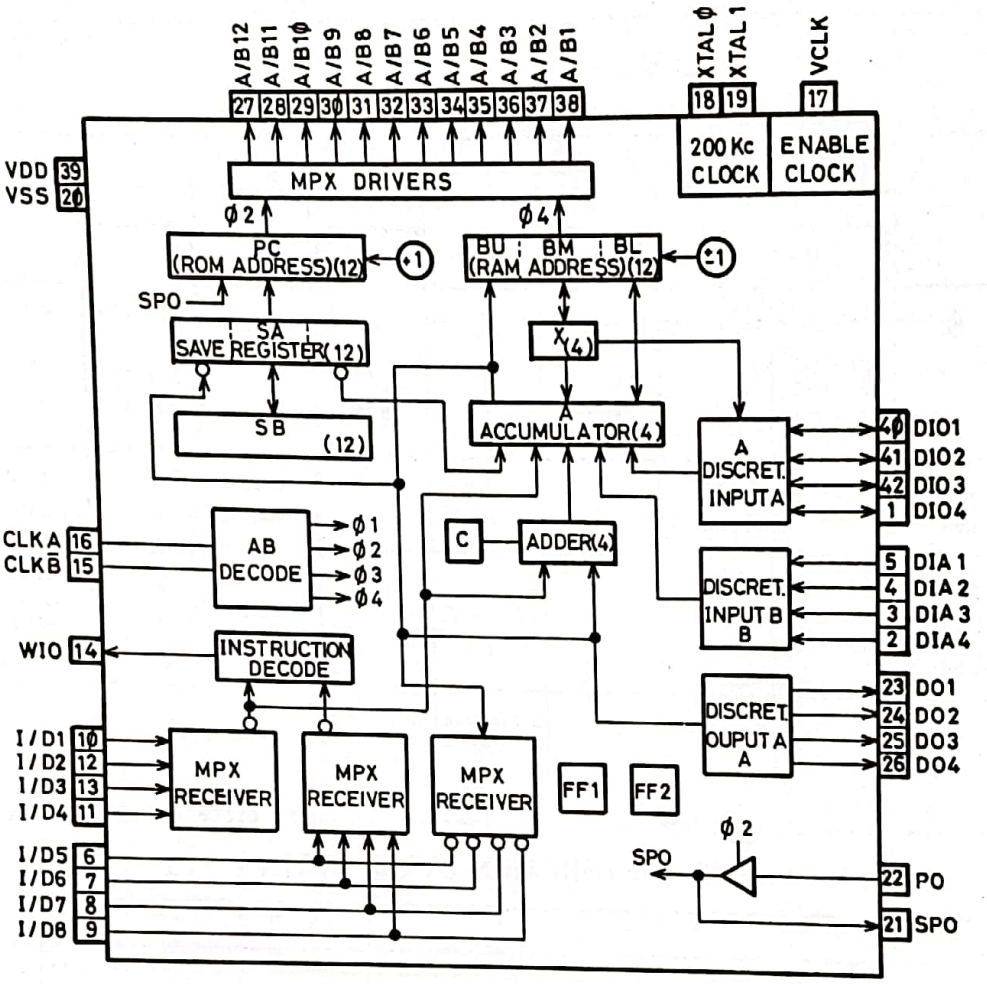
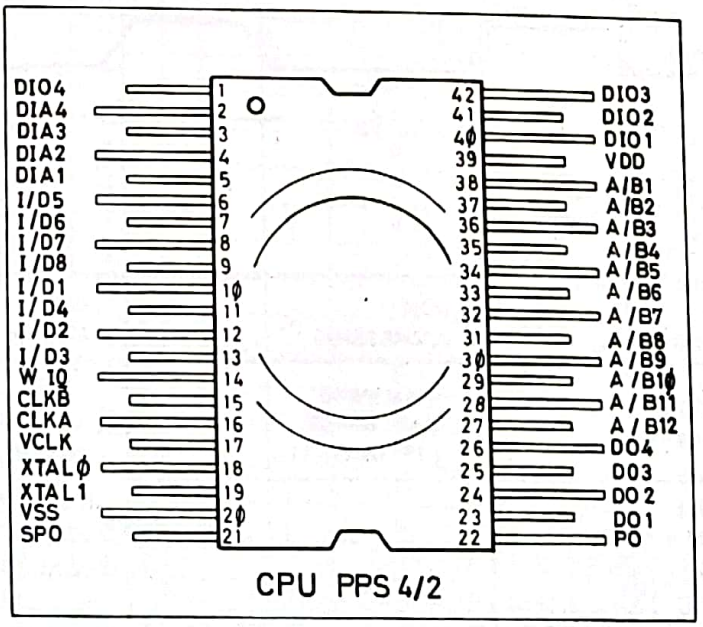
CPU / PPS-4/2 / PN 11660



VDD=-12V

VSS=+5V



CPU PPS 4/2

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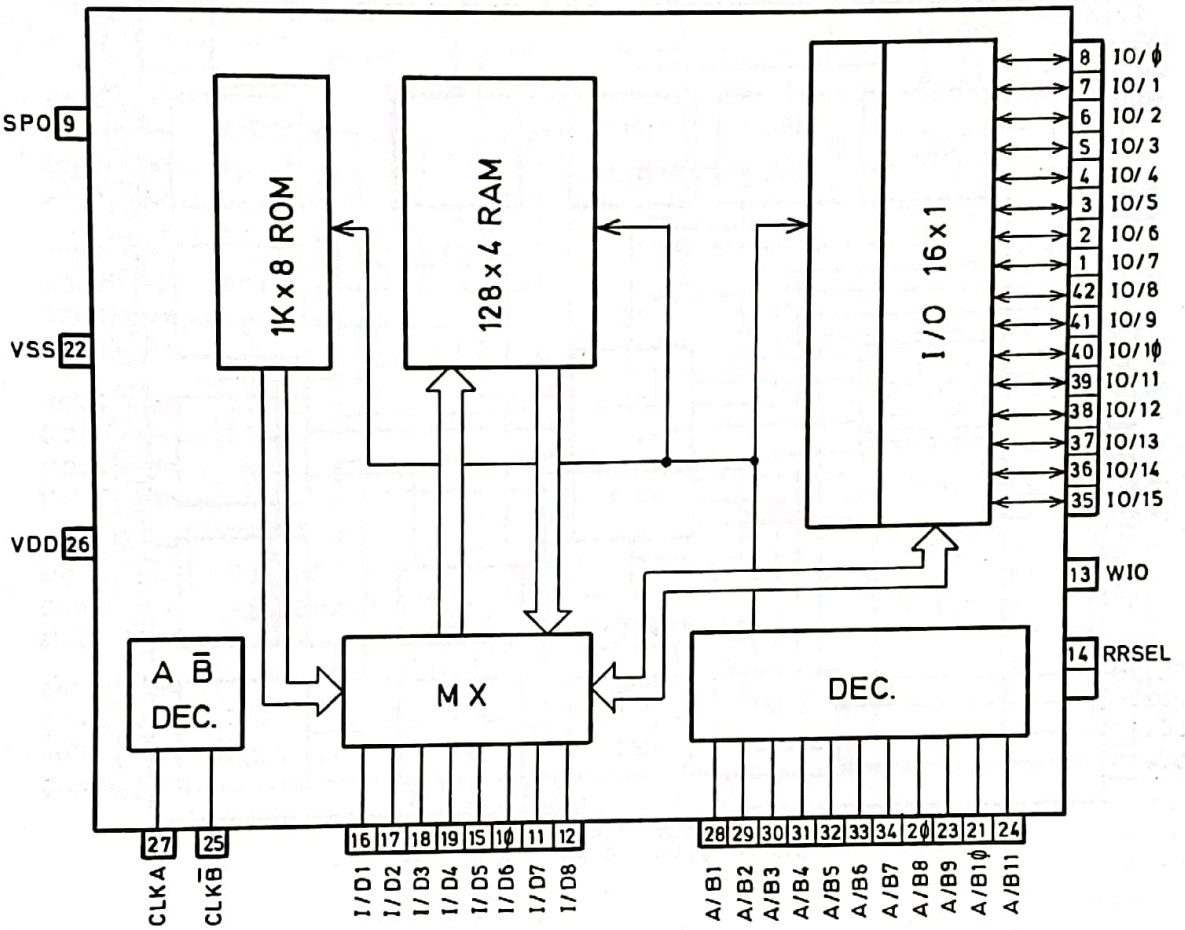
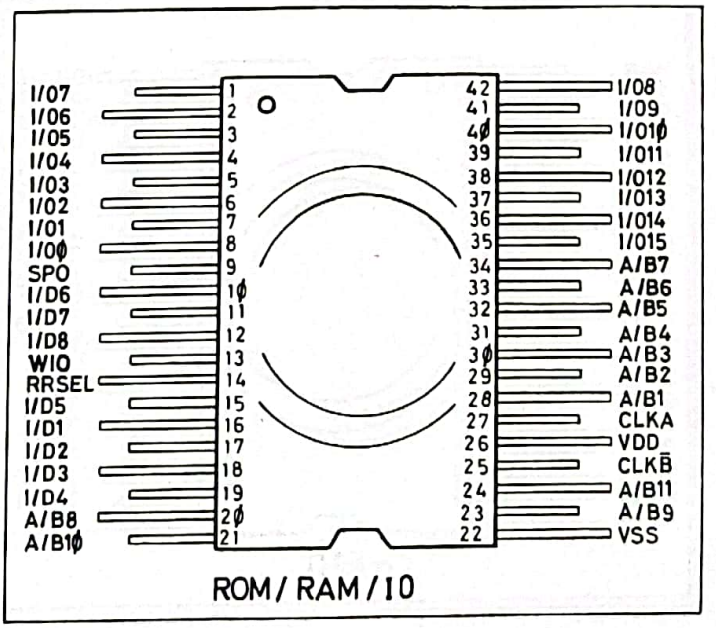
ROM/RAM/I-O A 2361-62
A 1761-62





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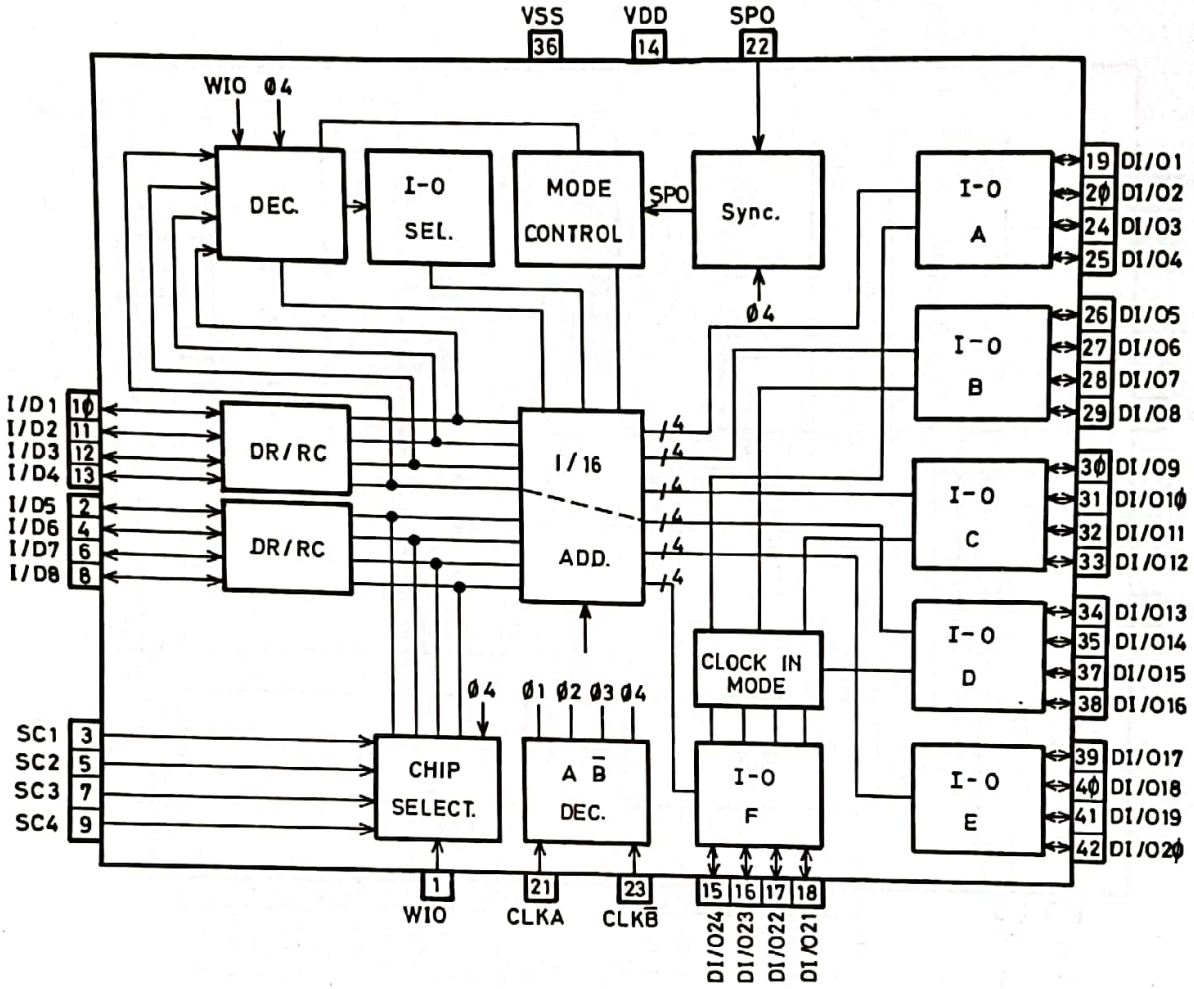
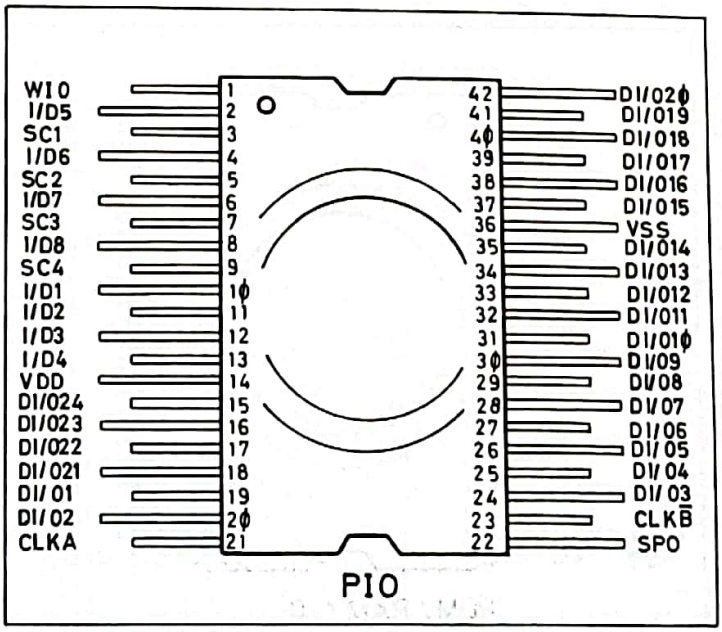
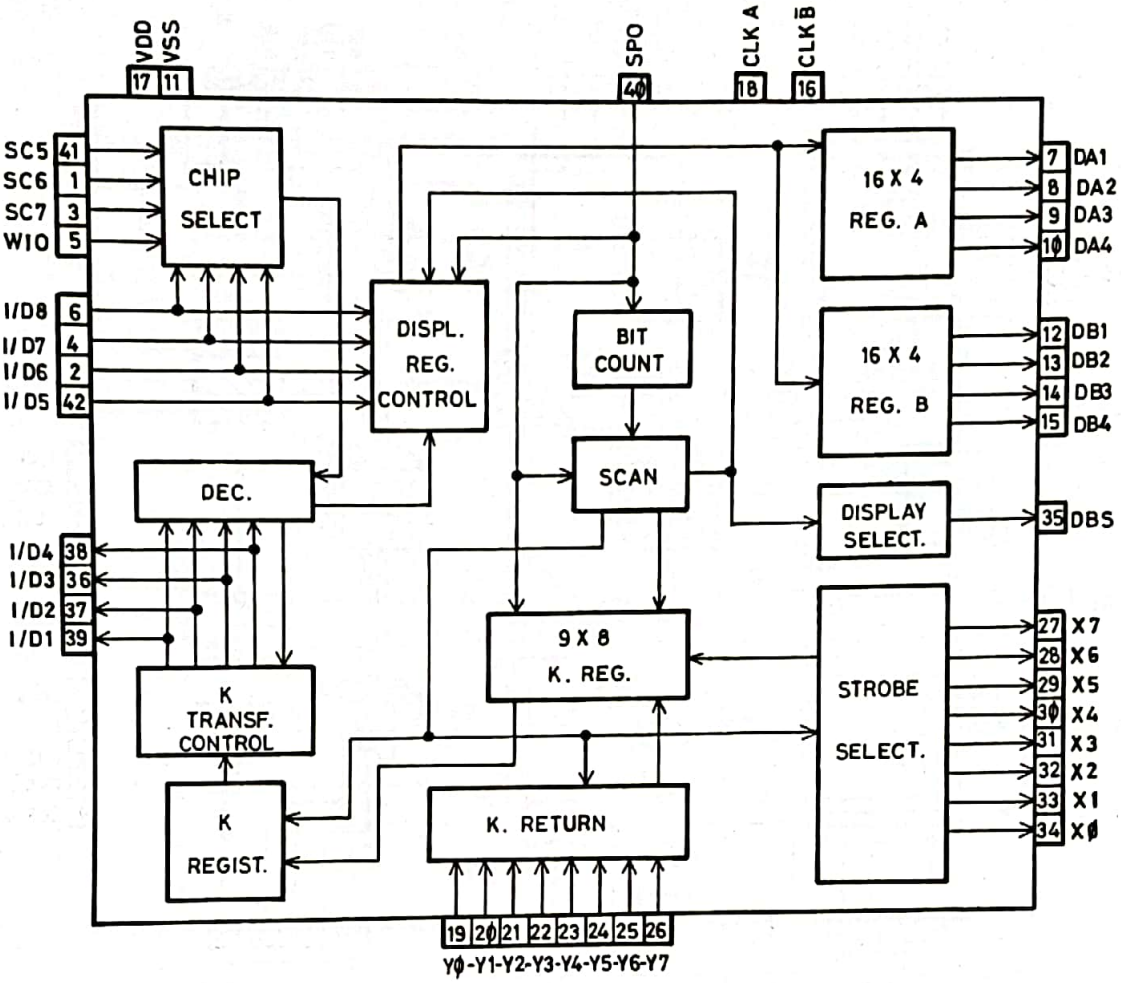
PIO/PN11696

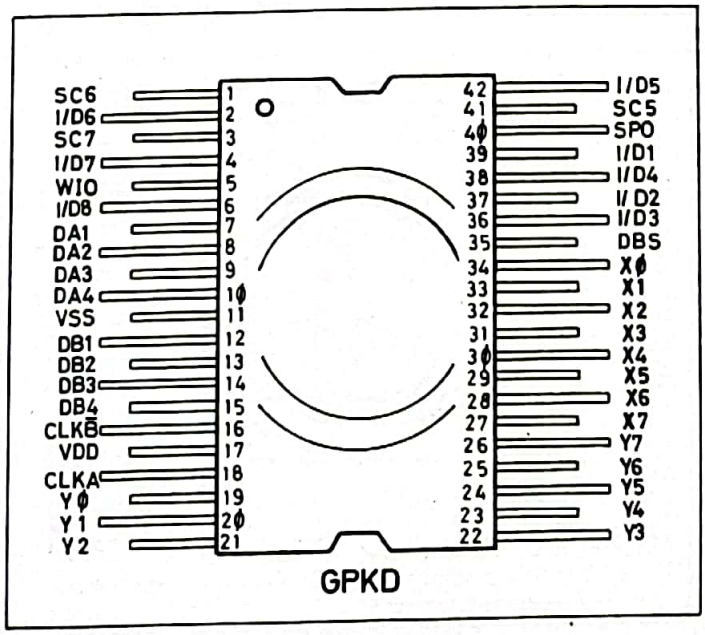




CamScanner

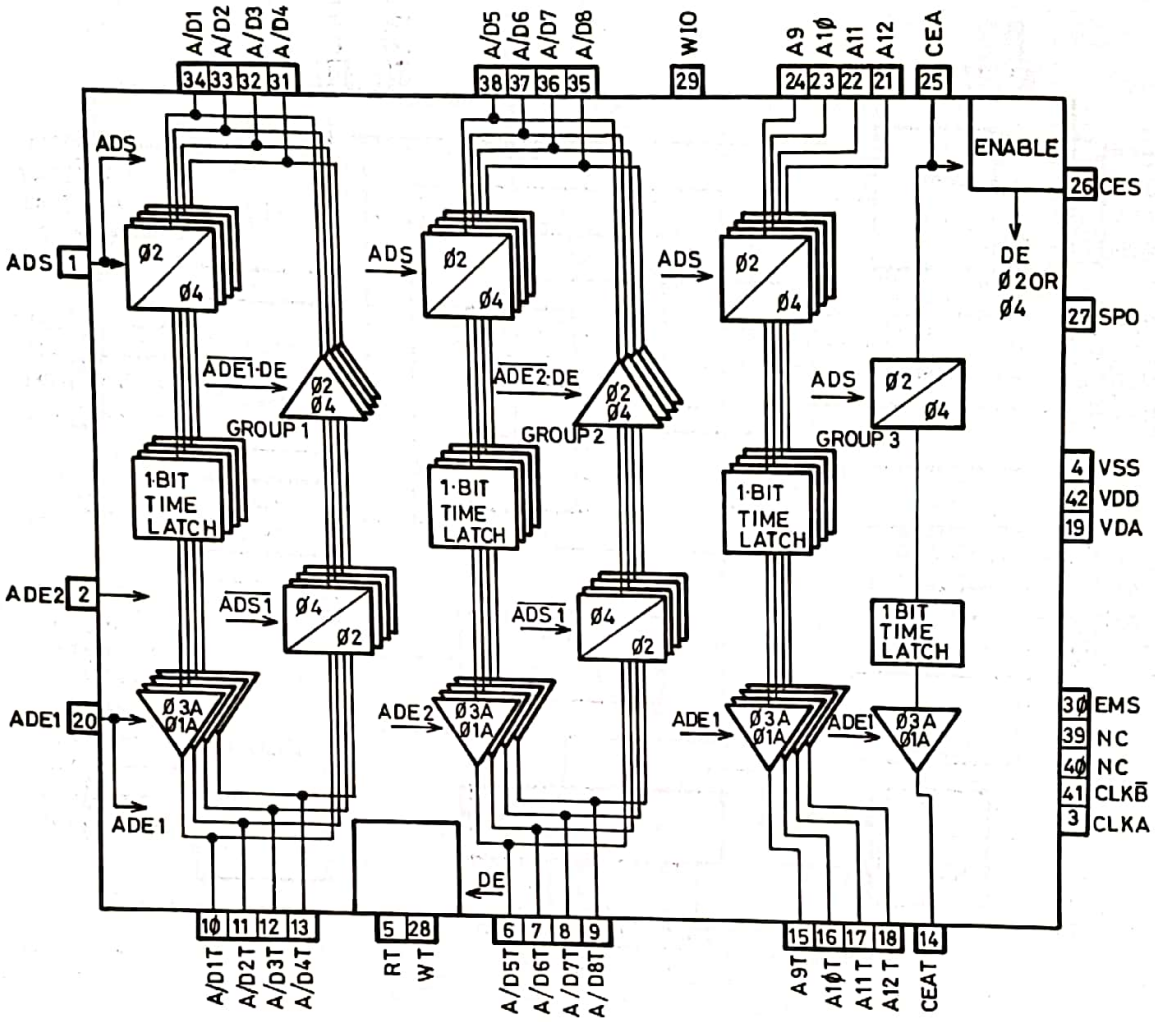
GPKD PN10788

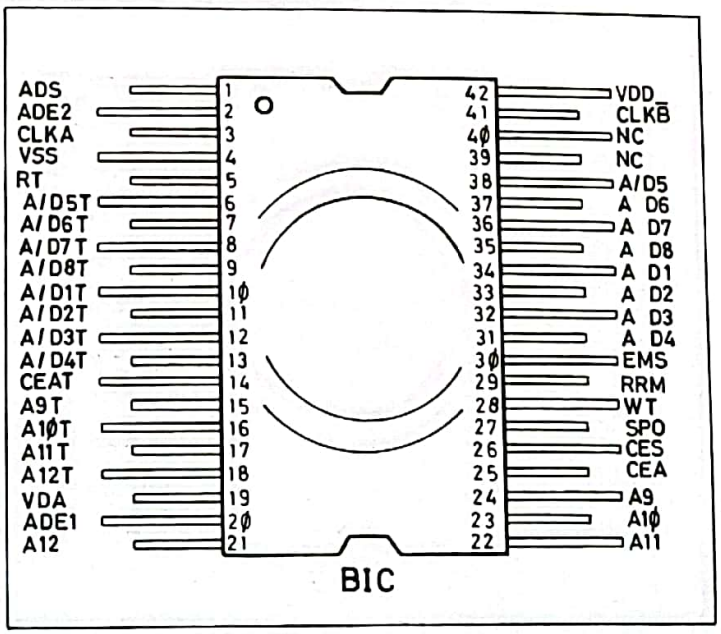




CamScanner

BIC/PN 10738





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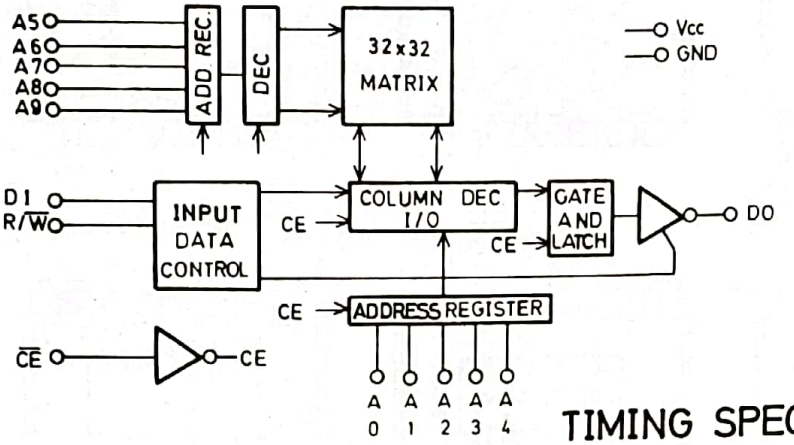
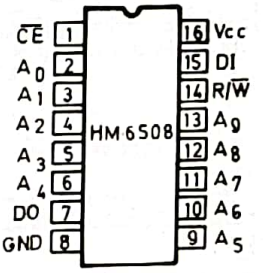
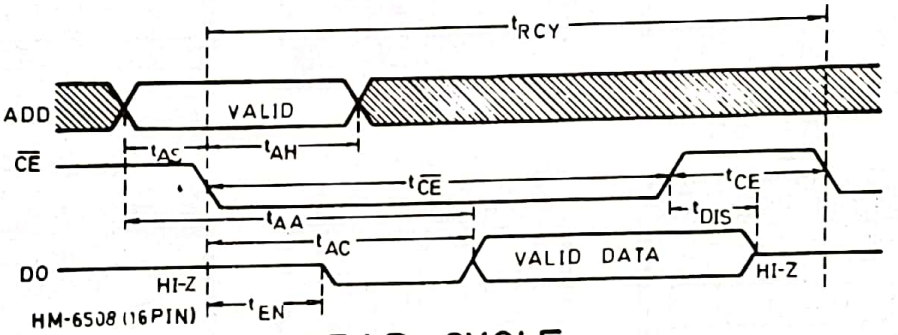
HM6508-9
RAM CMOS MEMORY

BLOCK DIAGRAM

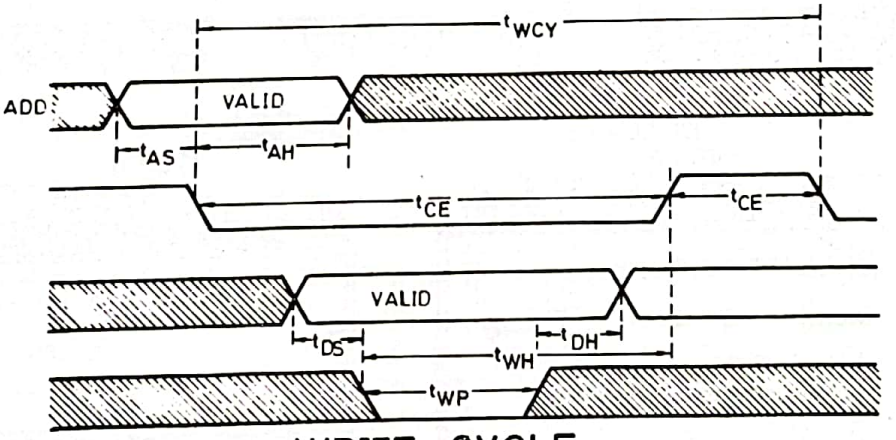




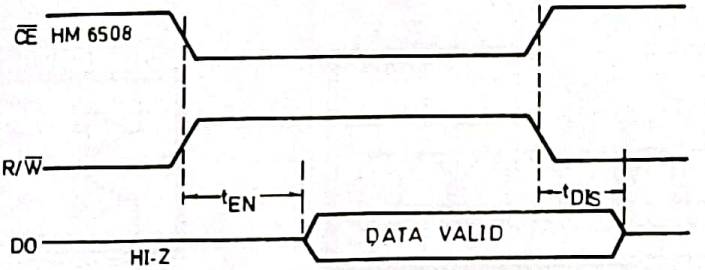
TIMING SPECIFICATION



READ CYCLE



WRITE CYCLE



TIMING ENABLE/DISABLE $t_R = t_F = 20ns$

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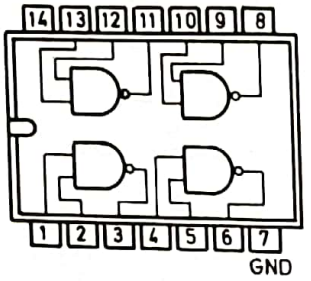
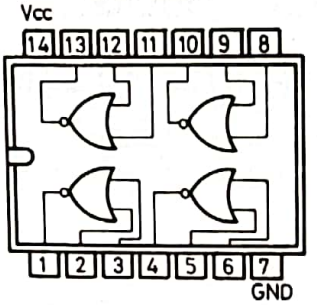
CHIPS UTILIZED

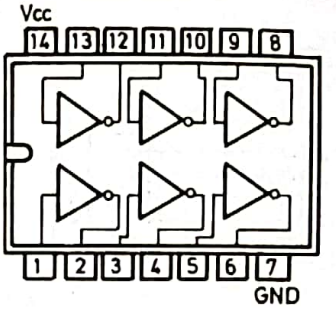
74C00
SN7400N
SM7403



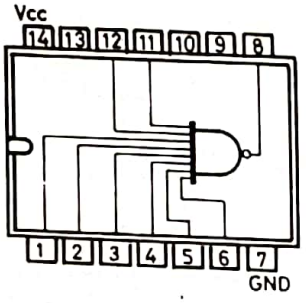
SN7402N



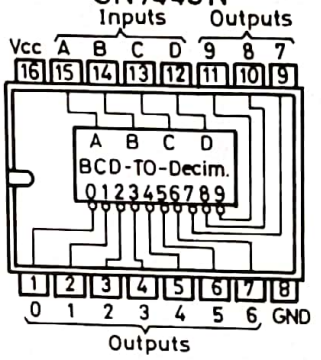
SN7404N



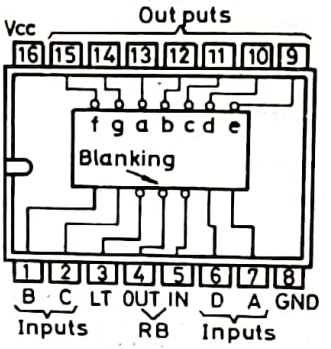
SN7430N



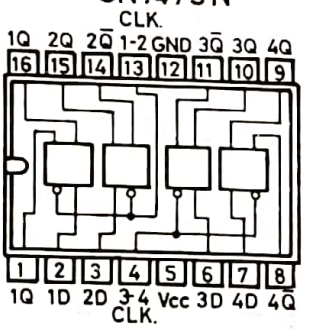
SN7445N



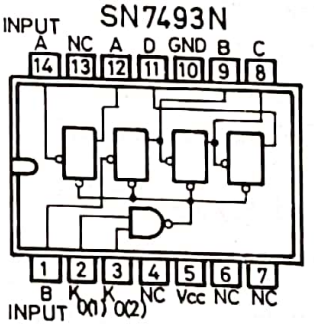
SN7448N



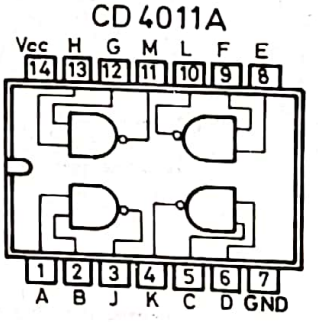
SN7475N



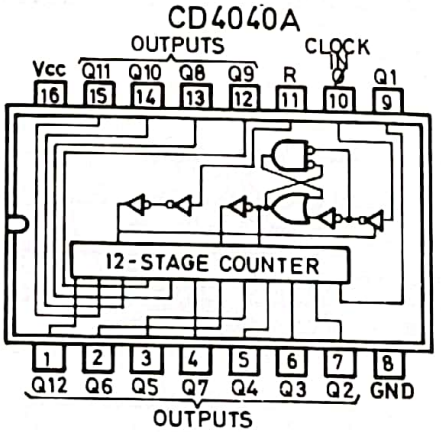
SN7493N



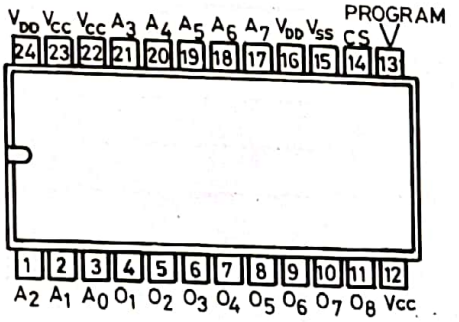
CD 4011A



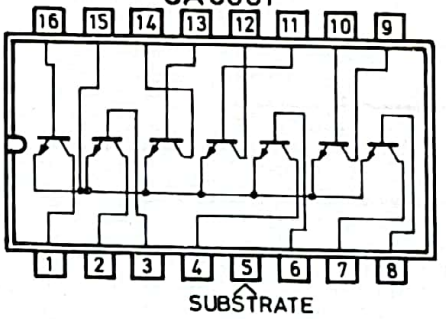
CD4040A



1702 A



CA 3081



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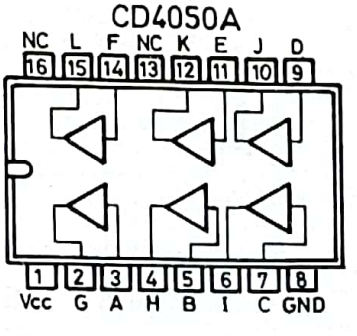

$V_{CC} = V_{SS}$ $GND = V_{DA}$

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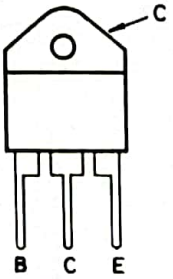
COMPONENTS UTILIZED



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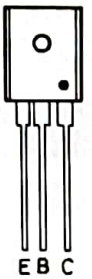

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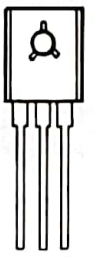

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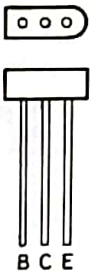
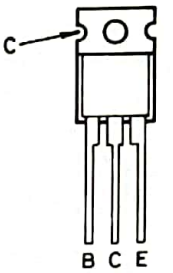


SC107.
SC109
2N 4291



TIP132
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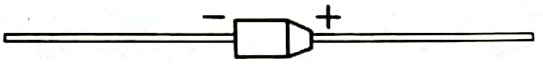
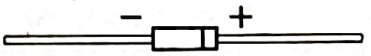
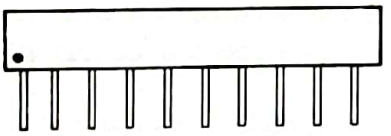
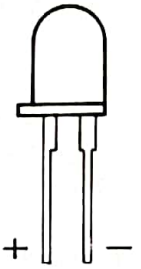
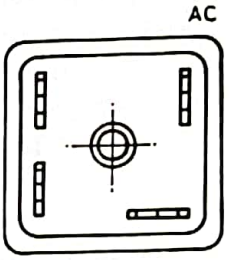
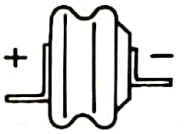




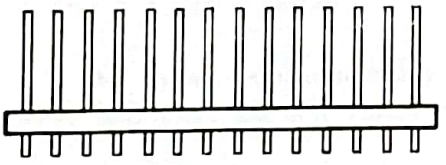


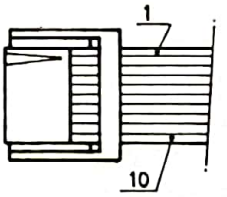


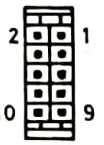




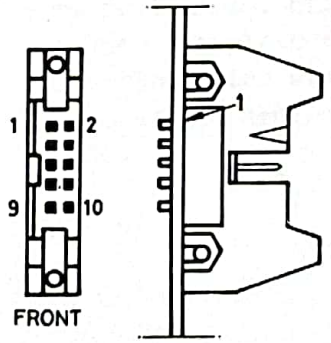
CONNECTORS



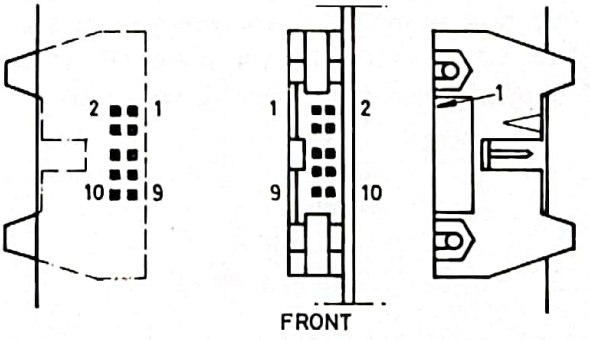




FEMALE SOCKET TRANSITION



ANSLEY WITH RIGHT CONTACTS



ANSLEY WITH STRAIGHT CONTACTS

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SECTION 7

RAM MEMORY MAP

The first of the tables in this section, represents the RAM memory organisation map. This organisation refers both to the RAM CMOS memory and to the RAM working memory. The two RAM systems are exactly alike, inasmuch as their capacity and data distribution are concerned. The RAM CMOS memory is intended solely to memorize all the data during the time the machine is switched off, and to recover all the information for the working RAM at the end of the Self-Check routine.

On the bottom line of the table, we have specified the displays which will represent the data given in the table, and naturally in accordance with the area selected.

The tables bearing titles **AREA Ø TO F** show directly the data which will be represented in each area, and the format of these tables correspond perfectly to the actual aspect they will have in the lite-box.

The values indicated in some RAM positions (memory map, columns 2 and A), are constants and make it possible to recognize the area in the memory which is being represented at any given moment. These constants, as can be seen on the map, are represented on the LEDs and decimal points of the 4 score counters.

The bytes represented by "Ø" form part of the counters and totalizers, and this is the value with which they leave our works.

The positions shown by "X" are adjustable, some of which can be altered with the machine itself, and others by means of the Alter RAM program or the mini-printer; the constants indicated on line F determine the time (complement) required to read each group of 4 switches and the values indicated are the standard ones. If in any particular model different values are required, they will be given in the respective SERVICE MANUAL.

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RAM MEMORY ORGANIZATION

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0				WORK REGISTER													0
1	PLAYFIELD					⑥	Ⓔ	—Ⓕ—	WK	WK	※1	Ø Ø Ø Ø Ø SERIAL Nº OF PRINTER					1
2	※1 CREDIT LIMIT	WK	WK	※F MODEL					WK	WK	※3	Ø Ø Ø Ø Ø PRODUCTION Nº					2
3	Ø Ø Ø Ø TIME AT GAME OVER								Ø	Ø	Ø TIME	Ø Ø Ø Ø Ø IN PLAY					3
4	③ FREE PLAY	④ EX.BALL	SL UP HP ⑧ 10⁶	Ø Ø Ø Ø Ø PLAYER Nº 1					STATE ⓪ TILT PLAY	MATCH NUMBER	SL UP HP ⑨ 10⁶	Ø Ø Ø Ø Ø PLAYER Nº 2					4
5	CREDIT ②		SL UP HP ⑧ 10⁶	Ø Ø Ø Ø Ø PLAYER Nº 4					Nº OF PULSES	FIGURE Ⓓ	SL UP HP Ⓐ 10⁶	Ø Ø Ø Ø Ø PLAYER Nº 3					5
6	※6 1ºFREE	※5 PLAY	※C	Ø Ø Ø Ø Ø 1st HANDICAP					EX. BALL REG.	EX. PLAY REG.	※C	Ø Ø Ø Ø Ø 2nd HANDICAP					6
7	※8 2ºFREE	※2 PLAY	※C	Ø Ø Ø Ø Ø 4th HANDICAP					PLAY M. REG.	TRANSFER AREA	※C	Ø Ø Ø Ø Ø 3rd HANDICAP					7
8	※4 EXTRA	※4 BALL	※Ø	Ø Ø Ø Ø Ø 1st COIN REJECTOR					WK	T I M E R	※1	Ø Ø Ø Ø Ø 2nd COIN REJECTOR					8
9	※3 ADJ.	※F PLAY	※Ø	Ø Ø Ø Ø Ø DATE OF LAST RETURNS					WK		※Ø	Ø Ø Ø Ø Ø 3rd COIN REJECTOR					9
A	C1+1 2C 1 COIN	C2+2 BON. 2S	※Ø	Ø Ø Ø Ø Ø TOTAL OF EXTRA BALL					WK		※2	Ø Ø Ø Ø Ø TOTAL FREE PLAY					A
B	3rd REJECTOR	E. BALL MOD. 3 BALLS ⑤ REP. 5 BALLS	※Ø	Ø Ø Ø Ø Ø PLAY TOTALIZER						Ⓒ	※Ø	Ø Ø Ø Ø Ø SERVICE TOTAL					B
C	—	—	1st CONTACT READING					—	—	—	※3	Ø Ø Ø Ø Ø TOTAL RESERVE 1					C
D		COINCIDENCES									※4	Ø Ø Ø Ø Ø TOTAL RESERVE 2					D
E	BH ⑦	STATE OF CONTACTS						—	G.O. C3 C2 C1	TILT START ① S1 S2	※2	Ø Ø Ø Ø Ø TOTAL RESERVE 3					E
F	※A	※A PRESET	※A	※A CONTACT	※A	※A	※C TIME	※C	※3	※Ø	※1	Ø Ø Ø Ø Ø TOTAL RESERVE 4					F
READING ON	Ø EX.PLAY	1 EX.BALL CREDIT	2 LEDS	3 4 5 6 7 DISPLAYS 1st AND 4th PLAYERS					8 BALL-TILT GAME OVER	9 MATCH NUMBER	A LEDS	B C D E F DISPLAYS 2nd AND 3rd PLAYERS					

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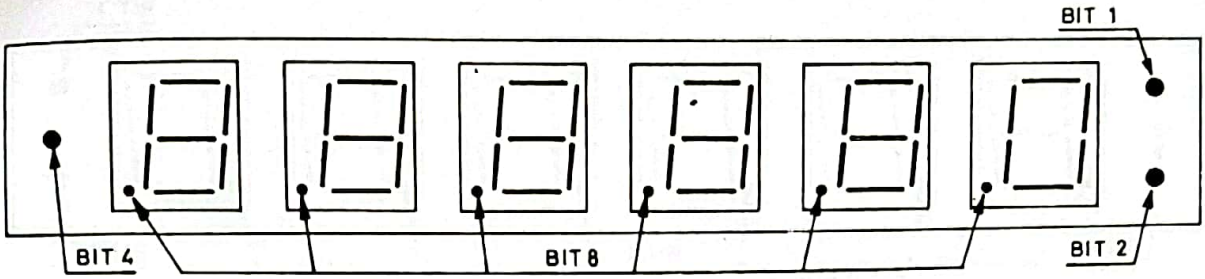

AREA 4

0	0 PLAYER	0	0 Nº 1	0	BIT 1 2 4 8	0 EXTRA GAMES	0 EXTRA BALLS
0	0 PLAYER	0	0 Nº 2	0	BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 GAME STATE TILT 8	5 6 7 8 4 9 3 2 1 0 MATCH NUMBER
0	0 PLAYER	0	0 Nº 3	0	BIT 1 2 4 8	—	—
0	0 PLAYER	0	0 Nº 4	0	BIT 1 2 4 8	0 CREDIT	

AREA 5

0	0 PLAYER	0	0 Nº 4	0	BIT 1 2 4 8	0 CREDIT	
0	0 PLAYER	0	0 Nº 3	0	BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 Nº IMPULSES TILT 8 *	5 6 7 8 4 9 3 2 1 0 DIGIT AFFECTED
0	0 PLAYER	0	0 Nº 2	0	BIT 1 2 4 8	—	—
0	0 PLAYER	0	0 Nº 1	0	BIT 1 2 4 8	0 EXTRA GAMES	0 EXTRA BALLS

* DATA FOR PROCESSOR CHECK

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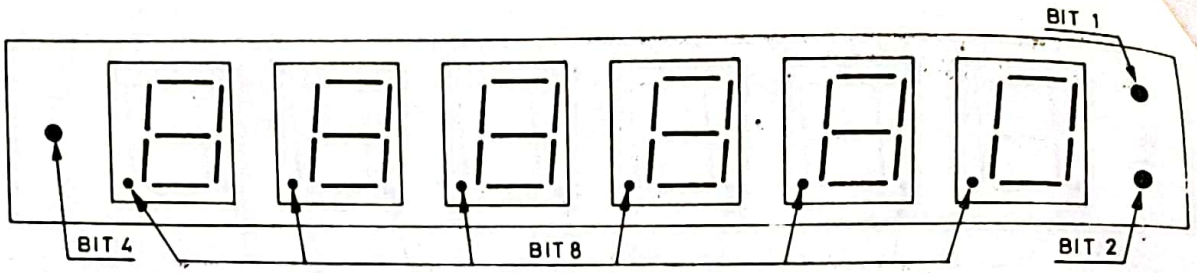


AREA 6

PLAYER	Nº 1	HANDICAP			BIT 1 2 4 8	1ST GAME BY SCORING	
PLAYER	Nº 2	HANDICAP			BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8 EX. BALL SW.	EX. PLAY SW.
PLAYER	Nº 3	HANDICAP			BIT 1 2 4 8	—	—
PLAYER	Nº 4	HANDICAP			BIT 1 2 4 8	2ND GAME BY SCORING	

ADJUSTABLE

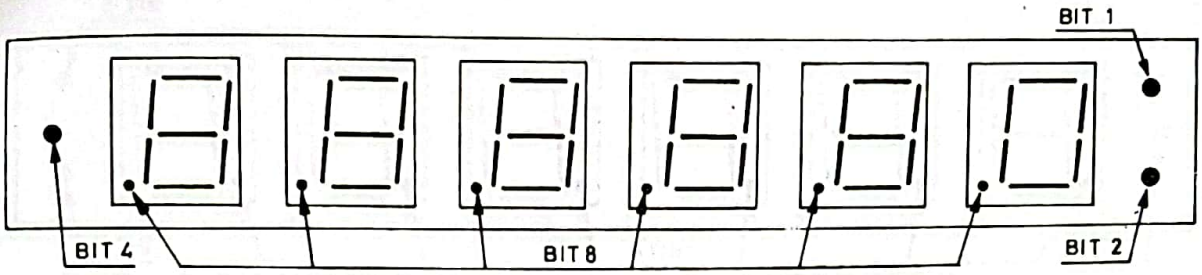
AREA 7

PLAYER	Nº 4	HANDICAP			BIT 1 2 4 8	2ND GAME BY SCORING	
PLAYER	Nº 3	HANDICAP			BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 PLAY TILT 8 MODE	* TRANSF. ZONE
PLAYER	Nº 2	HANDICAP			BIT 1 2 4 8	—	—
PLAYER	Nº 1	HANDICAP			BIT 1 2 4 8	1ST GAME BY SCORING	

* DATA FOR PROCESSOR CHECK

ADJUSTABLE

CamScanner



AREA 8

TOTAL COIN REJECTOR 1					BIT 1 2 4 8	EXTRA BALL BY SCORING	
TOTAL COIN REJECTOR 2					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	TIMER Ø
TOTAL COIN REJECTOR 3					BIT 1 2 4 8	—	—
LAST	COIN COLLECTION	DATE	OR	N°	BIT 1 2 4 8	GAME ADJUSTMENT	

ADJUSTABLE

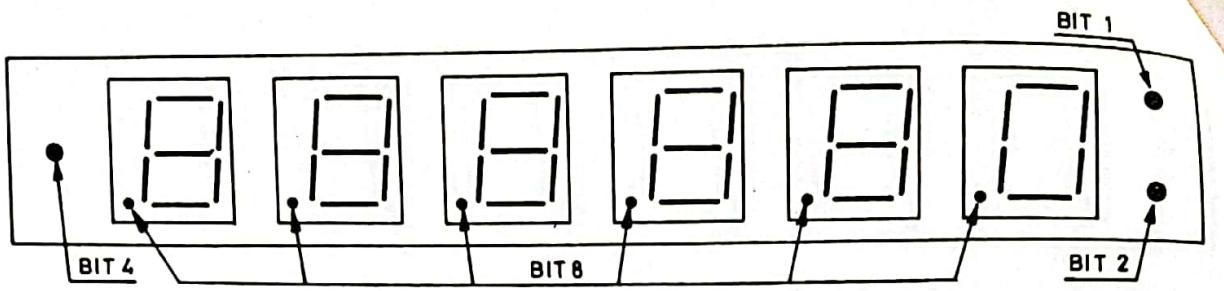
AREA 9

LAST	COIN COLLECTION	DATE	OR	N°	BIT 1 2 4 8	GAME ADJUSTMENT	
TOTAL COIN REJECTOR 3					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	TIMER 1*
TOTAL COIN REJECTOR 2					BIT 1 2 4 8	—	—
TOTAL COIN REJECTOR 1					BIT 1 2 4 8	EXTRA BALL BY SCORING	

* DATA FOR PROCESSOR CHECK

ADJUSTABLE

CamScanner



AREA A

	EXTRA BALL TOTAL				BIT 1 2 4 8	CASH BOX 1	CASH BOX 2
	FREE GAME TOTAL				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	TIMER 3*
	SERVICE GAME TOTAL				BIT 1 2 4 8	—	—
	GAMES PLAYED TOTAL				BIT 1 2 4 8	CASH BOX 3	GAME TYPE

ADJUSTABLE

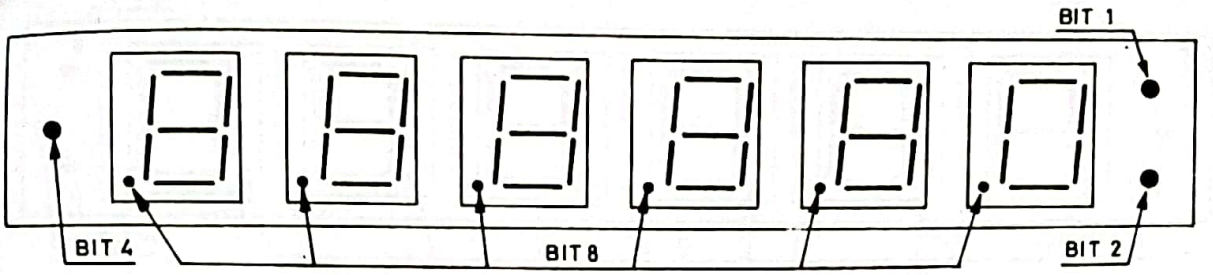
AREA B

	GAMES PLAYED TOTAL				BIT 1 2 4 8	CASH BOX 3	GAME TYPE
	SERVICE GAME TOTAL				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	TIMER 4*
	FREE GAME TOTAL				BIT 1 2 4 8	—	—
	GAMES PLAYED TOTAL				BIT 1 2 4 8	CASH BOX 1	CASH BOX 2

* DATA FOR PROCESSOR CHECK

ADJUSTABLE

CamScanner



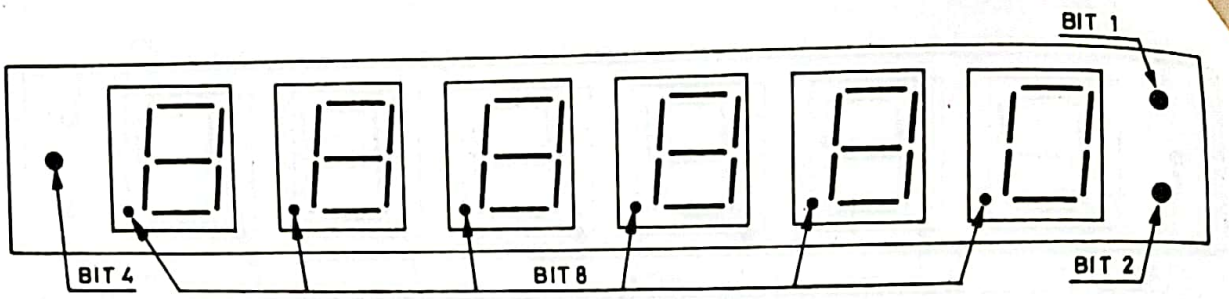
AREA C

INSTANT READING OF PLAY FIELD CONTACTS					BIT 1 2 4 8		
RESERVE	TOTALIZER 1				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO 5-6-7 TILT 8 GENERAL	CONTACTS
RESERVE	TOTALIZER 2				BIT 1 2 4 8	—	—
PLAY FIELD CONTACTS			COINCIDENCE Nº		BIT 1 2 4 8		

AREA D

PLAY FIELD CONTACTS			COINCIDENCE Nº		BIT 1 2 4 8		
RESERVE	TOTALIZER 2				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO 5-6-7 TILT 8 GEN. CONTACTS	COINCIDENCE
RESERVE	TOTALIZER 1				BIT 1 2 4 8	—	—
INSTANT READING OF PLAY FIELD CONTACTS					BIT 1 2 4 8		

CamScanner



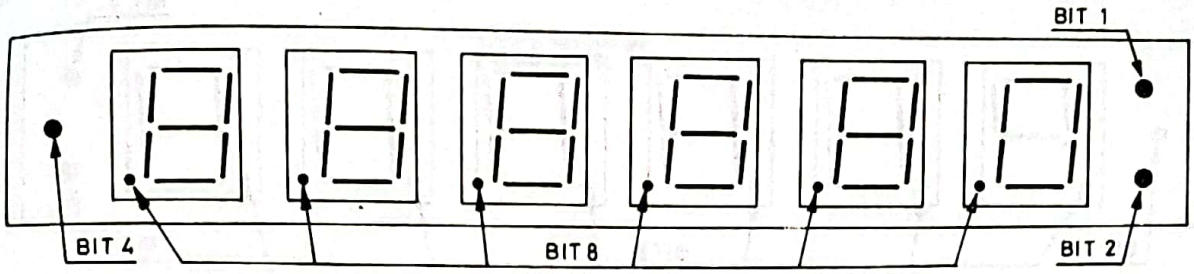
AREA E

PLAY FIELD CONTACT STATE					BIT 1 2 4 8		
RESERVE TOTALIZER 3					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	GEN. CONTACT STATE 0 1 2 3 4 5 6 7 8 9
RESERVE TOTALIZER 4					BIT 1 2 4 8	—	—
PLAY FIELD CONTACT TIME					BIT 1 2 4 8		

AREA F

PLAY FIELD CONTACT TIME					BIT 1 2 4 8		
RESERVE TOTALIZER 4					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	GEN. CONTACT TIME 0 1 2 3 4 5 6 7 8 9
RESERVE TOTALIZER 3					BIT 1 2 4 8	—	—
PLAY FIELD CONTACT STATE					BIT 1 2 4 8		

CamScanner



AREA ϕ

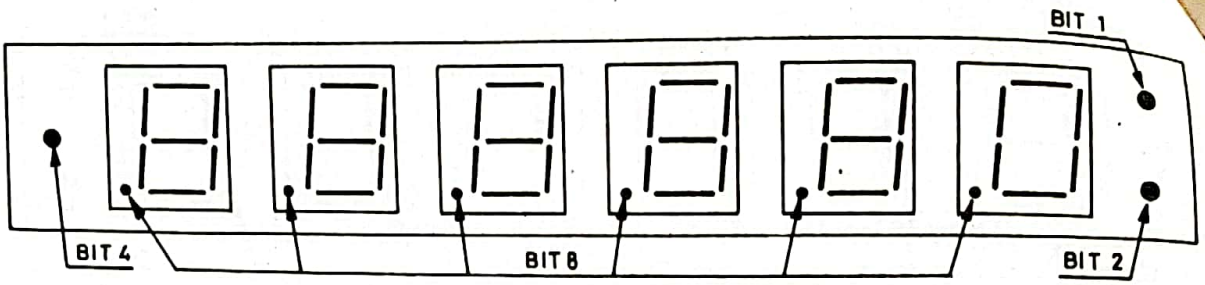
WORKING REGISTERS					BIT 1 2 4 8		*
WORKING REGISTERS					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	*
LAST PRINTER Nº					BIT 1 2 4 8	—	—
PLAY FIELD REGISTERS					BIT 1 2 4 8		

AREA 1

PLAY FIELD REGISTERS					BIT 1 2 4 8		
LAST PRINTER Nº					BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	
WORKING REGISTERS					BIT 1 2 4 8	—	— *
WORKING REGISTERS					BIT 1 2 4 8		*

* DATA FOR PROCESSOR CHECK

CamScanner



AREA 2

		MODEL			BIT 1 2 4 8	CREDIT LIMIT	
	SERIAL Nº				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO 5-6-7 TILT 8	5 6 7 8 4 3 9 2 1 0
	IN PLAY TIME				BIT 1 2 4 8	—	—
100.000 MIN.	GAME	OVER	TIME	10 MIN.	BIT 1 2 4 8 1 MIN.		0.01 MIN.

AREA 3

	GAME	OVER	TIME		BIT 1 2 4 8		
	IN PLAY TIME				BIT 1 2 4 8	BALL IN PLAY 0 1 2 3 4 GO. 5-6-7 TILT 8	5 6 7 8 4 3 9 2 1 0
	SERIAL Nº				BIT 1 2 4 8	—	—
		MODEL			BIT 1 2 4 8	CREDIT LIMIT	

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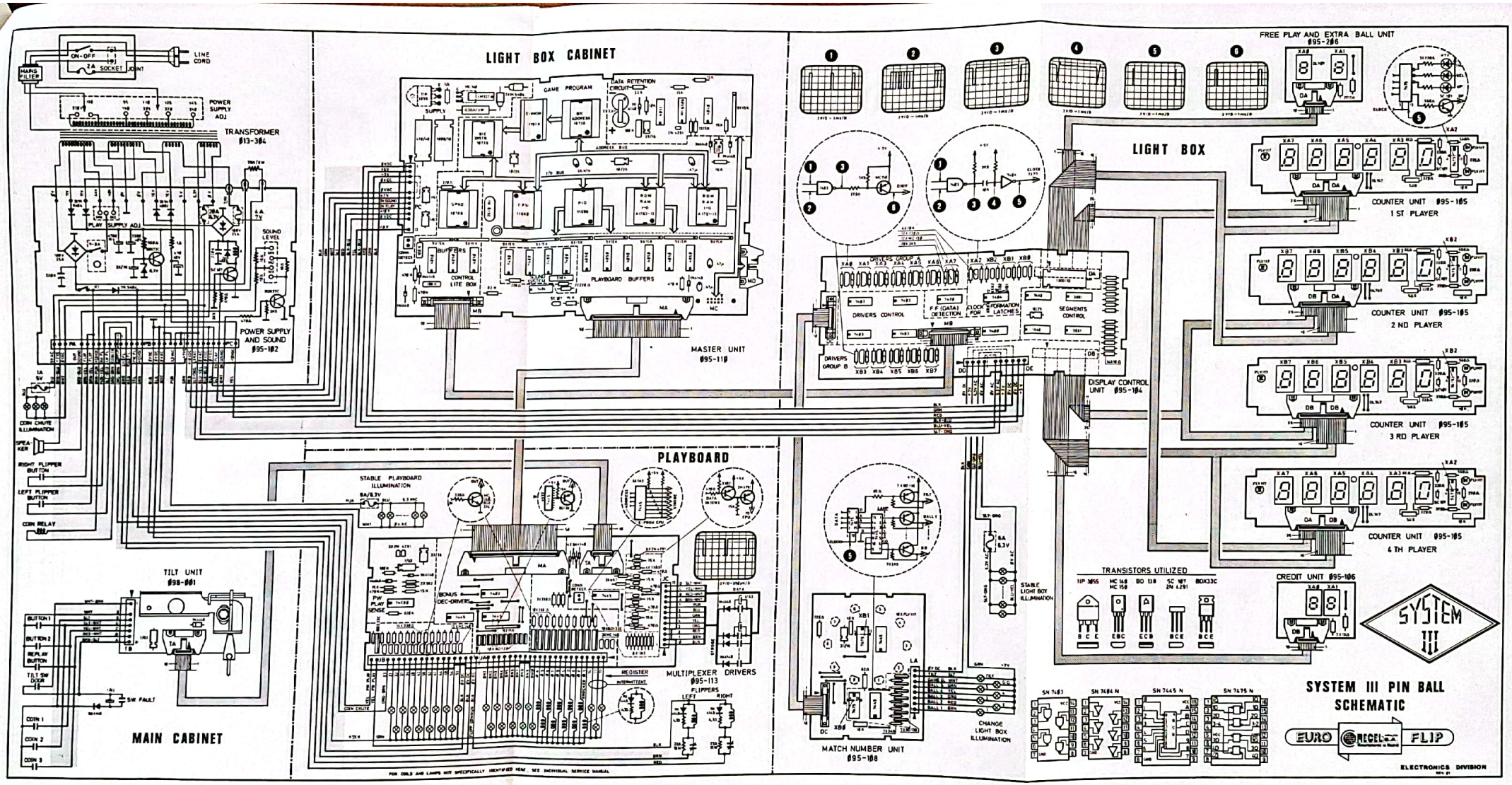
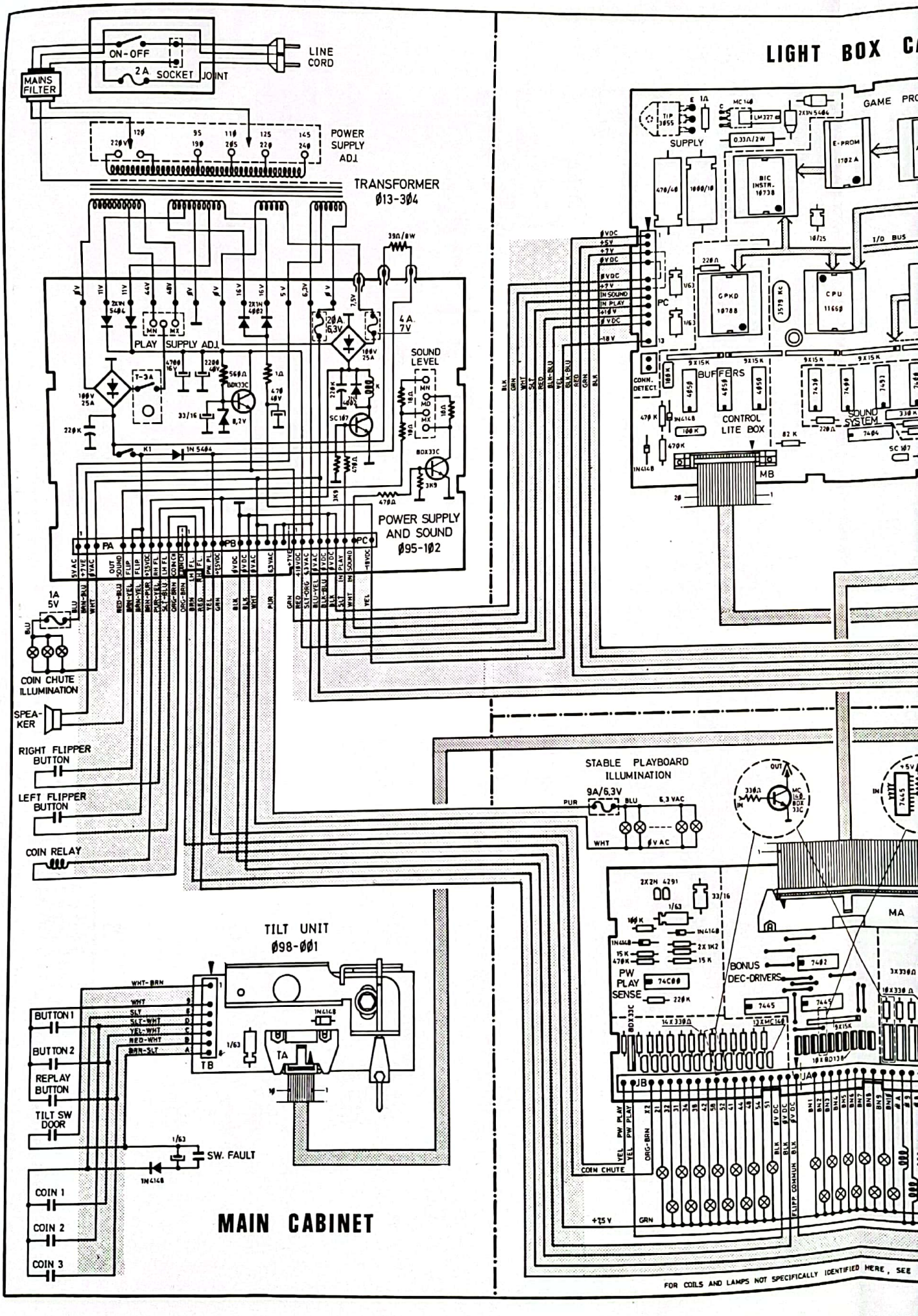
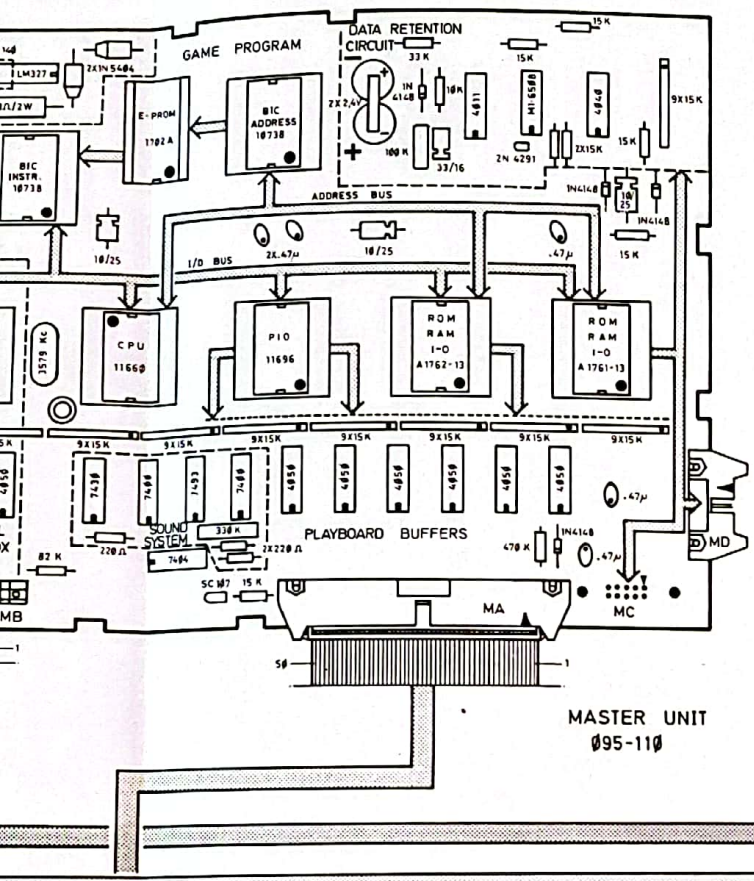

LIGHT BOX CABINET
MAIN CABINET
PLAYBOARD
LIGHT BOX
FREE PLAY AND EXTRA BALL UNIT
$95-286
TRANSFORMER
$13-384
POWER SUPPLY AND SOUND
$95-102
MASTER UNIT
$95-118
DISPLAY CONTROL UNIT $95-104
COUNTER UNIT $95-105
1 ST PLAYER
2 ND PLAYER
3 RD PLAYER
4 TH PLAYER
CREDIT UNIT $95-106
TILT UNIT
$98-801
MULTIPLEXER DRIVERS
$95-113
MATCH NUMBER UNIT
$95-108
TRANSISTORS UTILIZED
SYSTEM III PIN BALL SCHEMATIC
EURO FLIP
ELECTRONICS DIVISION

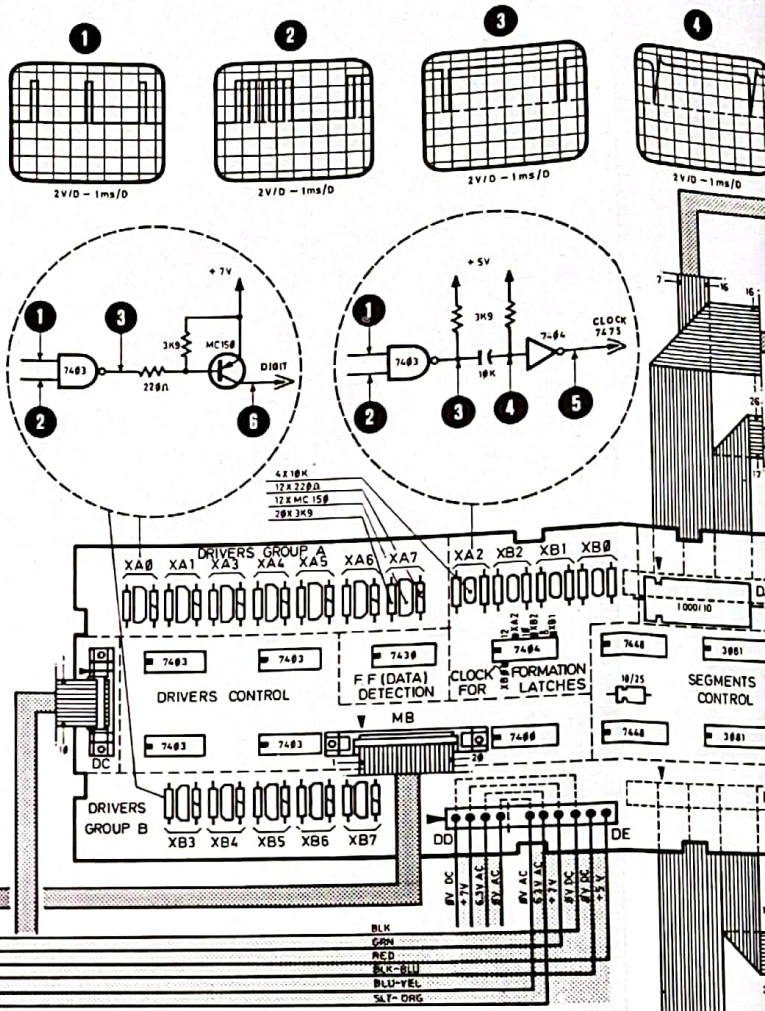
CamScanner

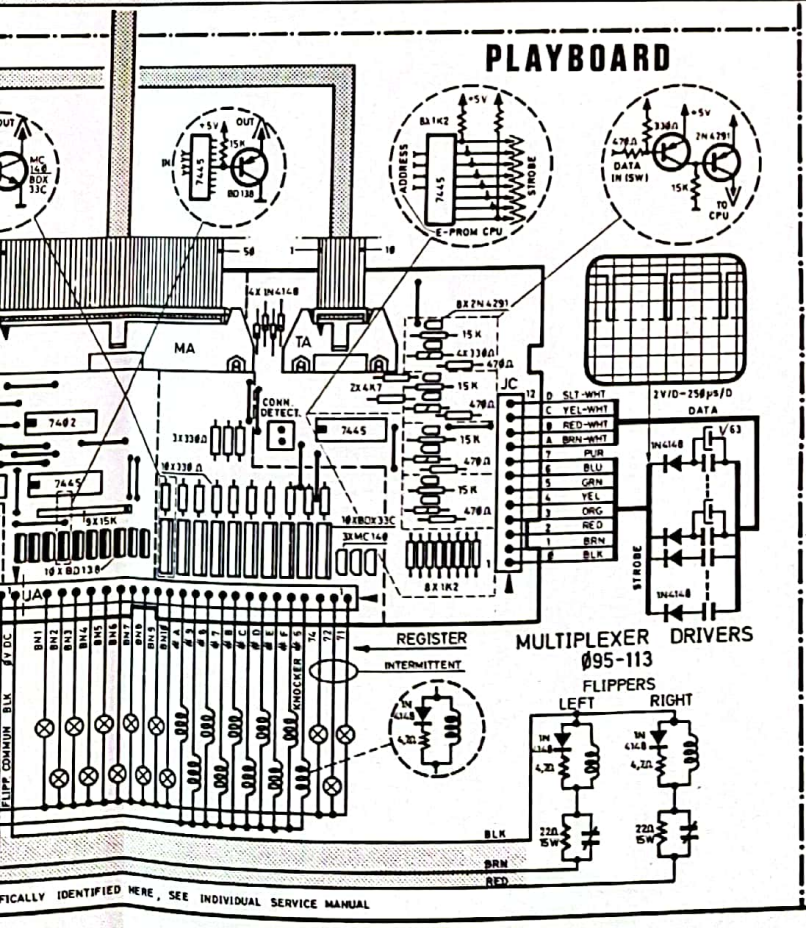

LIGHT BOX C
MAINS FILTER
ON-OFF
2A
SOCKET
JOINT
LINE CORD
POWER SUPPLY ADJ.
TRANSFORMER Ø13-3Ø4
PLAY SUPPLY ADJ.
SOUND LEVEL
POWER SUPPLY AND SOUND Ø95-1Ø2
PA
PB
PC
1A 5V
COIN CHUTE ILLUMINATION
SPEAKER
RIGHT FLIPPER BUTTON
LEFT FLIPPER BUTTON
COIN RELAY
TILT UNIT Ø98-ØØ1
BUTTON 1
BUTTON 2
REPLAY BUTTON
TILT SW DOOR
SW. FAULT
COIN 1
COIN 2
COIN 3
TB
TA
MAIN CABINET
GAME PRO
SUPPLY
E-PROM 1702 A
BIC INSTR. 1Ø738
GPKD 1Ø788
CPU 1166Ø
I/O BUS
BUFFERS
CONTROL LITE BOX
SOUND SYSTEM
CONN. DETECT.
MB
STABLE PLAYBOARD ILLUMINATION
9A/6,3V
PW PLAY SENSE
BONUS DEC-DRIVERS
MA
JB
JA
COIN CHUTE
FOR COILS AND LAMPS NOT SPECIFICALLY IDENTIFIED HERE, SEE

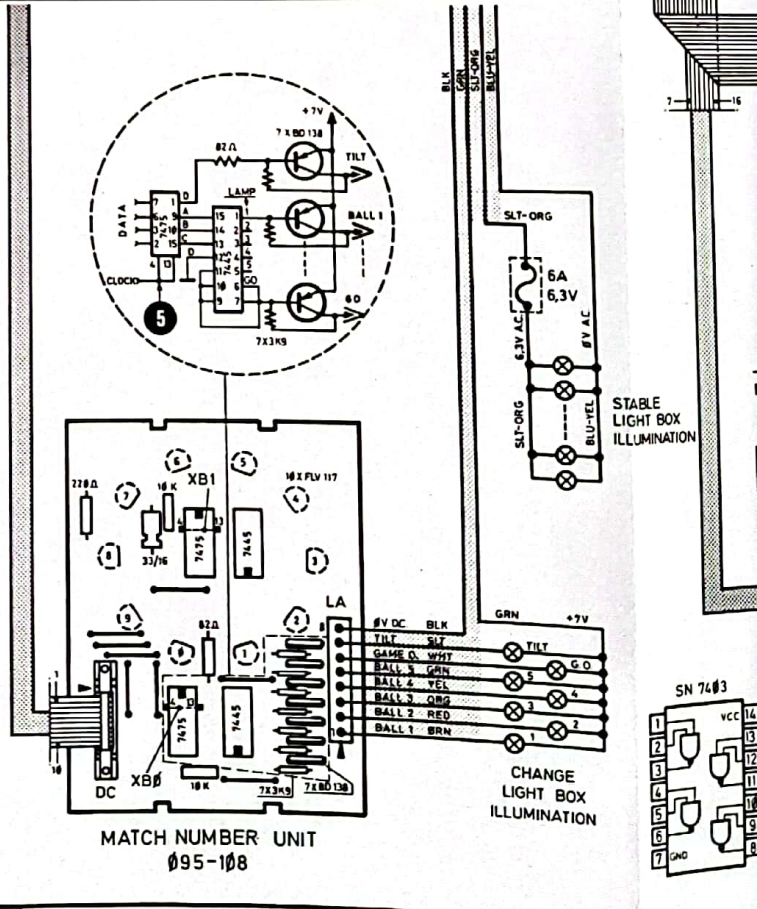
LIGHT BOX CABINET



MASTER UNIT
Ø95-11Ø

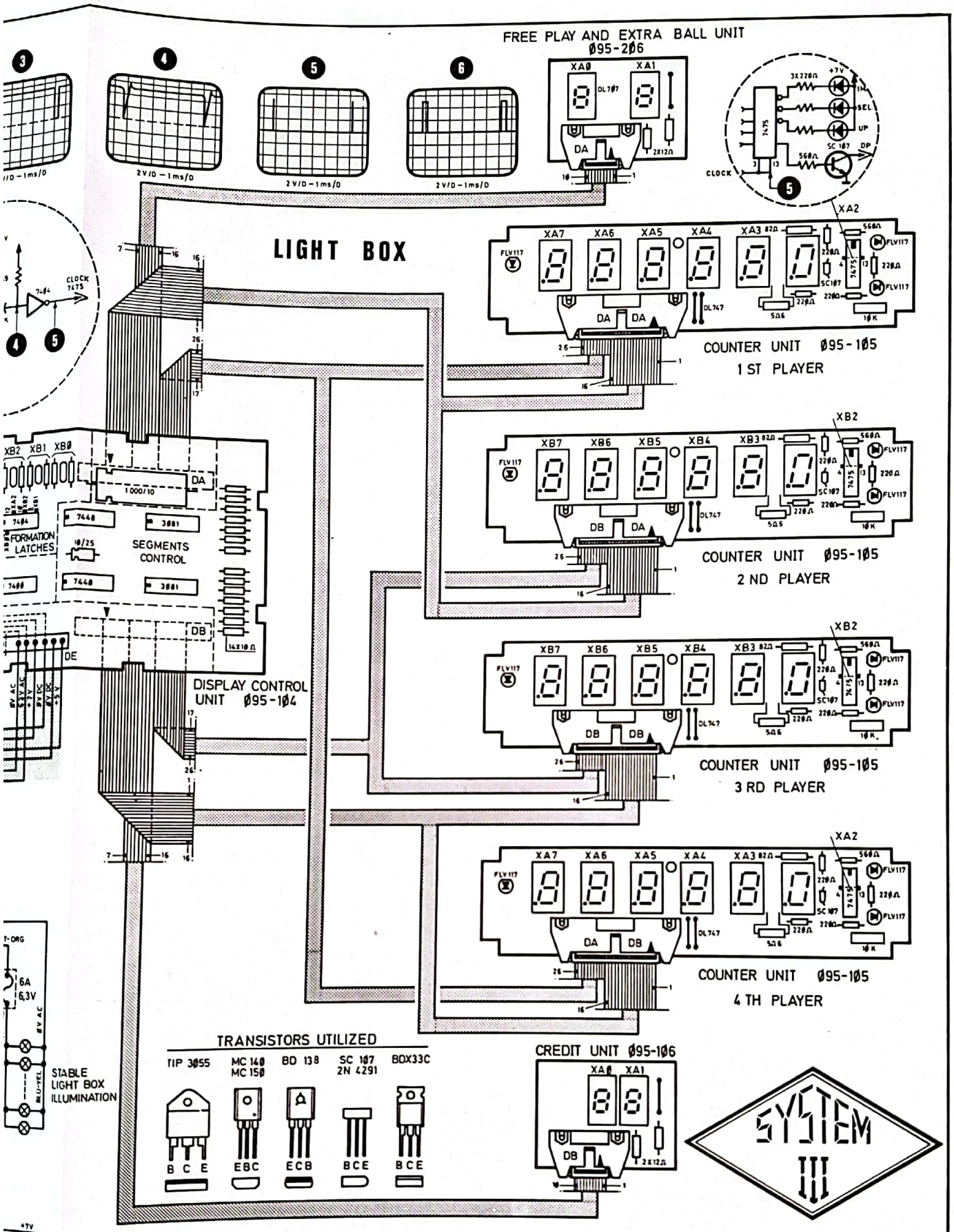




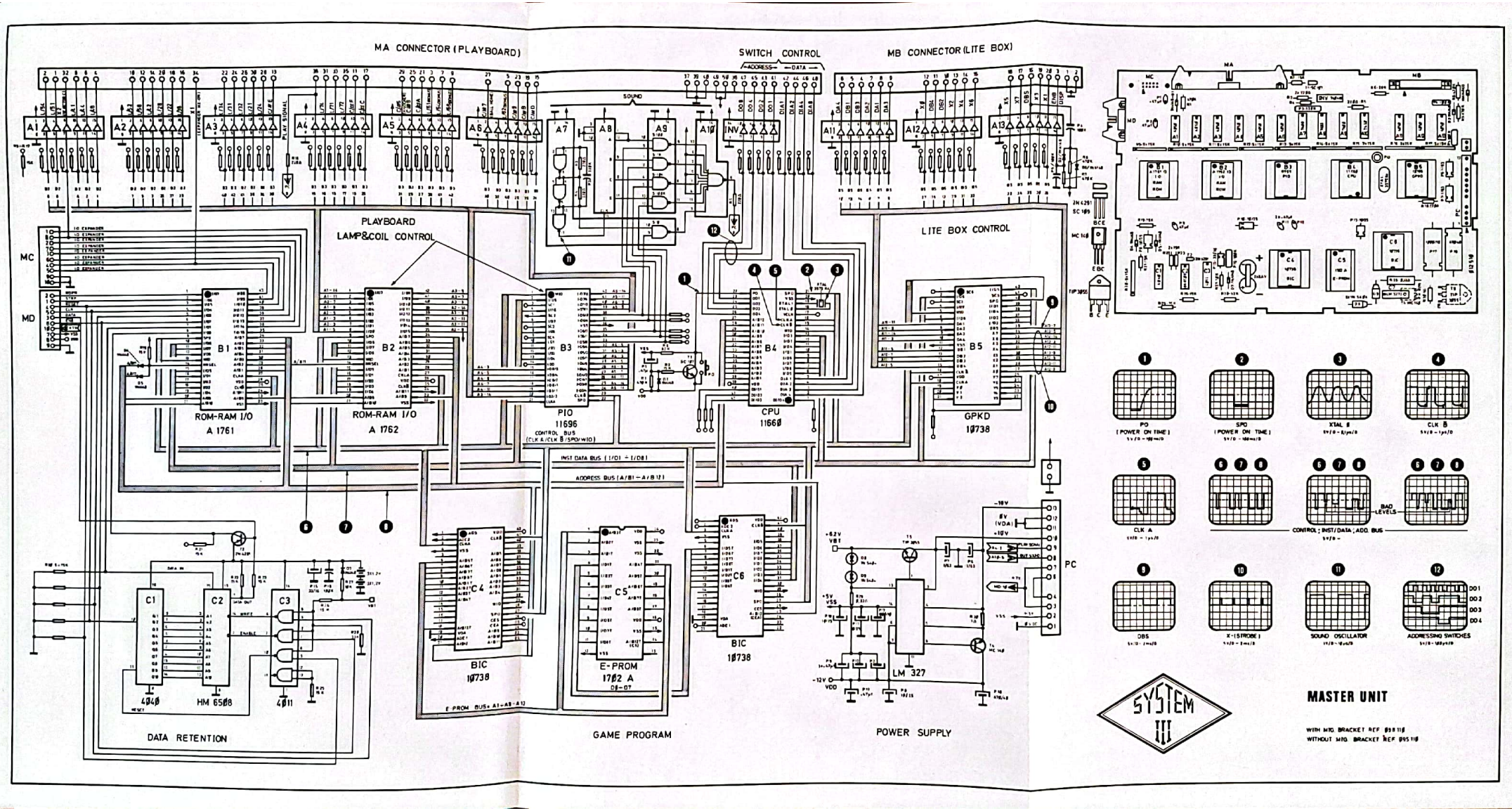


FICALLY IDENTIFIED HERE, SEE INDIVIDUAL SERVICE MANUAL

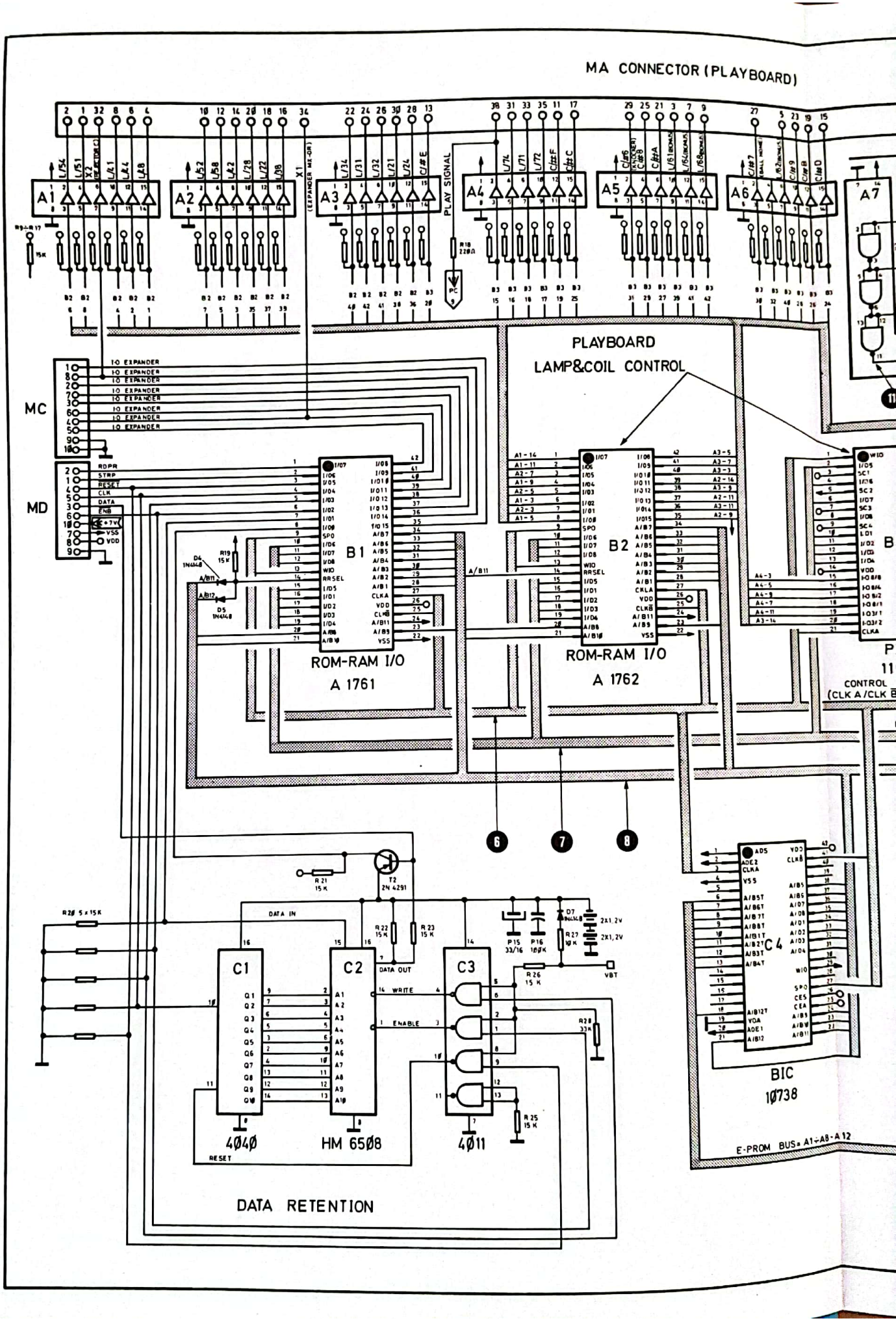
CamScanner


FREE PLAY AND EXTRA BALL UNIT
Ø95-2Ø6
LIGHT BOX
COUNTER UNIT Ø95-1Ø5
1 ST PLAYER
COUNTER UNIT Ø95-1Ø5
2 ND PLAYER
COUNTER UNIT Ø95-1Ø5
3 RD PLAYER
COUNTER UNIT Ø95-1Ø5
4 TH PLAYER
DISPLAY CONTROL UNIT Ø95-1Ø4
SEGMENTS CONTROL
FORMATION LATCHES
CREDIT UNIT Ø95-1Ø6
TRANSISTORS UTILIZED
TIP 3Ø55
MC 14Ø
MC 15Ø
BD 138
SC 1Ø7
2N 4291
BOX33C
STABLE LIGHT BOX ILLUMINATION
SN 74Ø3
SN 74Ø4 N
SN 7445 N
SN 7475 N
SYSTEM III
SYSTEM III PIN BALL
SCHEMATIC
EURO
RECEL
FLIP
ELECTRONICS DIVISION
REV Ø1

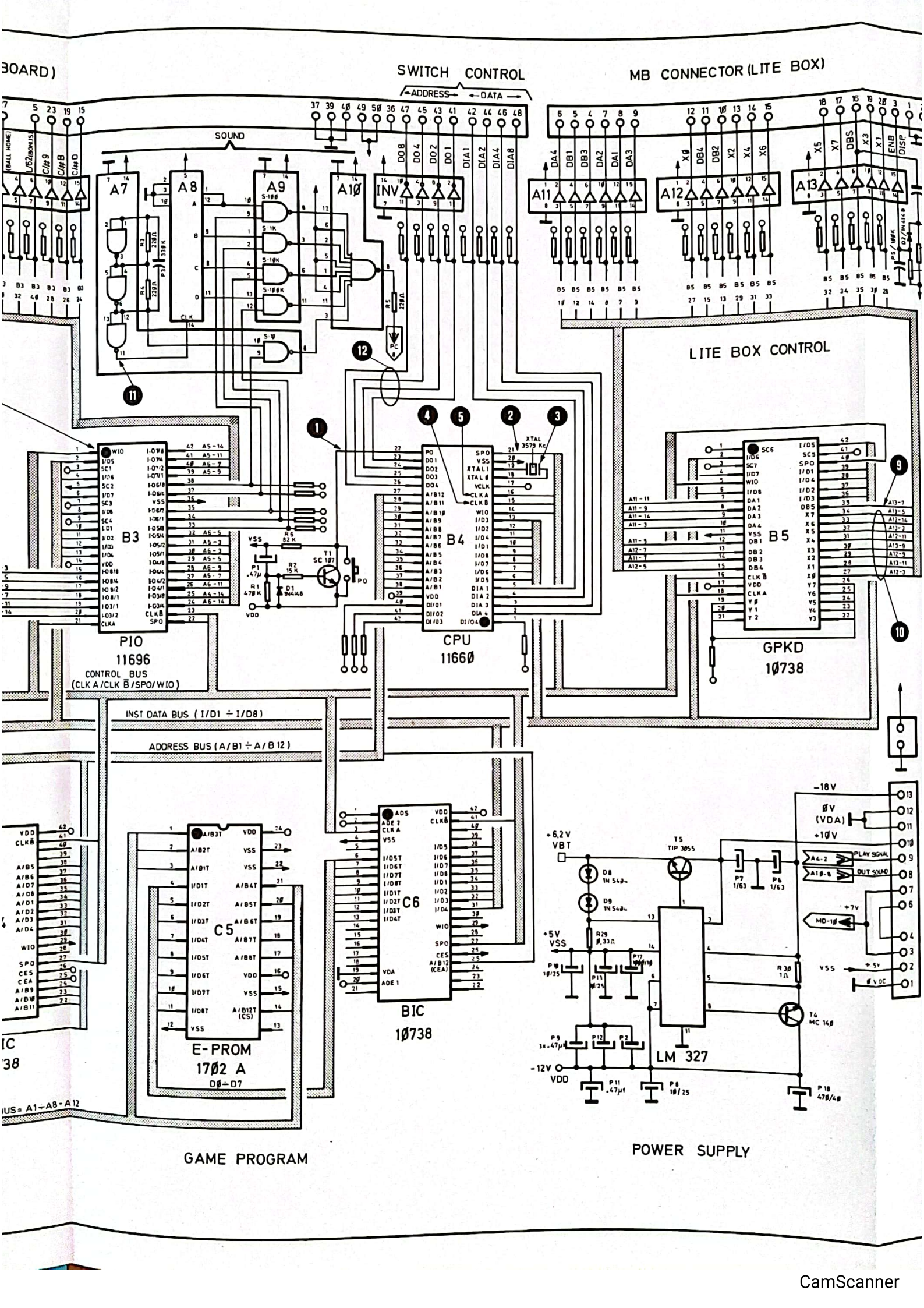
CamScanner


MA CONNECTOR (PLAYBOARD)
SWITCH CONTROL
ADDRESS
DATA
MB CONNECTOR (LITE BOX)
SOUND
PLAYBOARD
LAMP&COIL CONTROL
LITE BOX CONTROL
MC
MD
ROM-RAM I/O
A 1761
ROM-RAM I/O
A 1762
PIO
11696
CONTROL BUS
(CLK A/CLK B/SPO/WIO)
CPU
11660
GPKD
10738
INST DATA BUS (I/O1 – I/O8)
ADDRESS BUS (A/B1 – A/B12)
BIC
10738
E-PROM
1702 A
BIC
10738
LM 327
PC
4040
HM 6508
4011
DATA RETENTION
GAME PROGRAM
POWER SUPPLY
PO
(POWER ON TIME)
SPO
(POWER ON TIME)
XTAL B
CLK B
CLK A
BAD LEVELS
CONTROL ; INST/DATA ; ADD. BUS
OBS
X-(STROBE)
SOUND OSCILLATOR
ADDRESSING SWITCHES
SYSTEM III
MASTER UNIT
WITH MTG. BRACKET REF 895118
WITHOUT MTG. BRACKET REF 895116

CamScanner

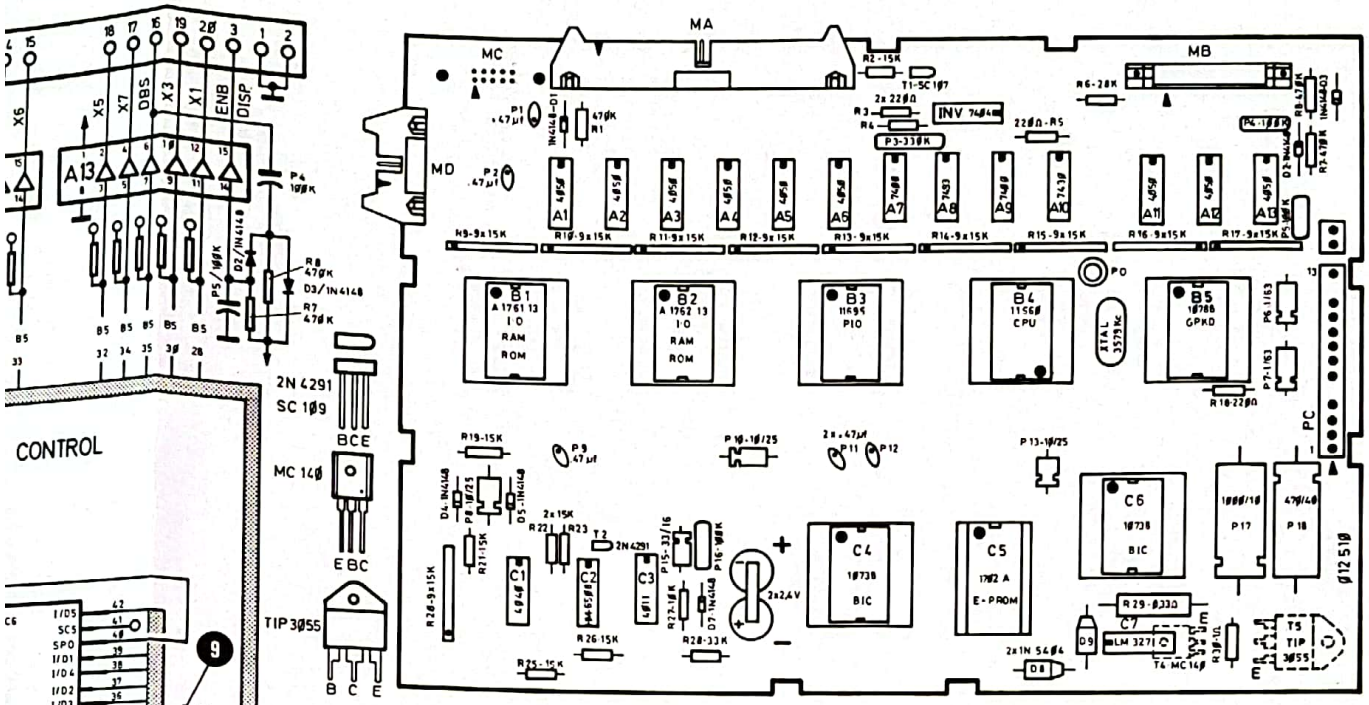

MA CONNECTOR (PLAYBOARD)
PLAYBOARD
LAMP&COIL CONTROL
PLAY SIGNAL
MC
MD
I-O EXPANDER
RDPR
STRB
RESET
CLK
DATA
ENB
+7V
VSS
VDD
ROM-RAM I/O
A 1761
B1
ROM-RAM I/O
A 1762
B2
BIC
1Ø738
C4
DATA IN
DATA OUT
WRITE
ENABLE
C1
C2
C3
4Ø4Ø
HM 65Ø8
4Ø11
RESET
DATA RETENTION
E-PROM BUS= A1÷A8-A12
CONTROL
(CLK A/CLK B)

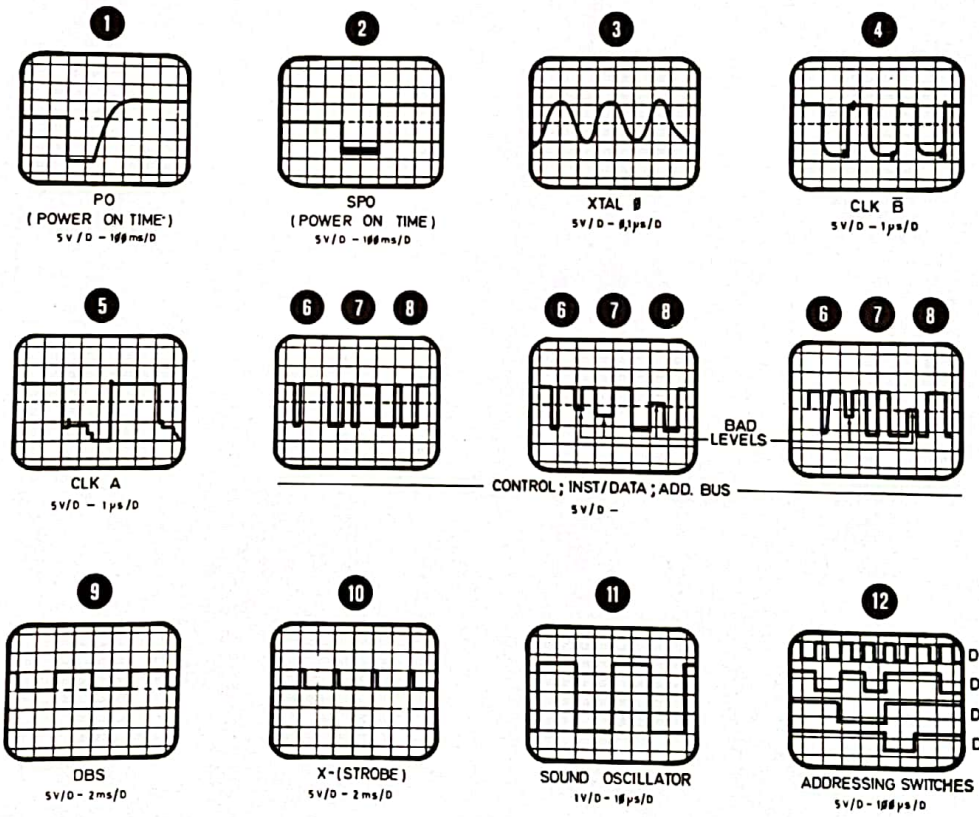
CamScanner



BOARD)
SWITCH CONTROL
ADDRESS
DATA
MB CONNECTOR (LITE BOX)
SOUND
A7
A8
A9
A10
INV
A11
A12
A13
LITE BOX CONTROL
B3
PIO
11696
CONTROL BUS
(CLK A/CLK B̄/SPO/WIO)
B4
CPU
11660
XTAL 3579 Kc
B5
GPKD
10738
INST DATA BUS (I/D1 ÷ I/D8)
ADDRESS BUS (A/B1 ÷ A/B12)
C5
E-PROM
1702 A
D0÷D7
C6
BIC
10738
-18V
0V (VDA)
+10V
+6,2V VBT
T5 TIP 3055
PLAY SIGNAL
OUT SOUND
+7V
MD-10
+5V VSS
-12V VDD
LM 327
T4 MC 140
BUS= A1÷A8-A12
GAME PROGRAM
POWER SUPPLY

(LITE BOX)





SYSTEM III

MASTER UNIT

WITH MTG. BRACKET REF. 098 110
WITHOUT MTG. BRACKET REF. 095 110

CamScanner